AV Mathematics-III for EC Engineering		Semester	3
Course Code	**BMATEC301**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express non-periodic functions to periodic functions using the Fourier series and Fourier transforms.
- Analyze signals in terms of Fourier transforms
- Develop the knowledge of solving differential equations and their applications in Electronics & Communication engineering.
- To find the association between attributes and the correlation between two variables

Teaching-Learning Process

Pedagogy (General Instructions):

These are sample Strategies, teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

Module-1: Fourier series and practical harmonic analysis

Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period 2π and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current.**(8 hours)**

(RBT Levels: L1, L2 and L3)

Module-2: Infinite Fourier Transforms

Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT), Fast Fourier transform (FFT). **(8 hours)**

(RBT Levels: L1, L2 and L3)

Module-3: Z Transforms

Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z- transforms. Application to difference equations. **(8 hours)**

(RBT Levels: L1, L2 and L3)

Module-4: Ordinary Differential Equations of Higher Order

Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems.Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations–Problems. Application of linear differential equations to L-C circuit and L-C-R circuit.**(8 hours)**

(RBT Levels: L1, L2 and L3)

Module-5: Curve fitting, Correlation, and Regressions

Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Coefficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation. **(RBT Levels: L1, L2 and L3)(8 hours)**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and field theory.
2. To use Fourier transforms to analyze problems involving continuous-time signals
3. To apply Z-Transform techniques to solve difference equations
4. Understand that physical systems can be described by differential equations and solve such equations
5. Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)

Text Books:

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig**: "Advanced Engineering Mathematics", John Wiley & Sons, 10thEd., 2018.

Reference Books:

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11thEd., 2017
2. **Srimanta Pal & Subodh C.Bhunia**: "Engineering Mathematics" Oxford University Press, 3rdEd., 2016.
3. **N.P Bali and Manish Goyal**: "A Textbook of Engineering Mathematics" Laxmi Publications, 10thEd., 2022.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw–Hill Book Co., New York, 6thEd., 2017.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", McGraw Hill Education(India) Pvt. Ltd 2015.
6. **H.K. Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication, 3rdEd.,2014.
7. **James Stewart: "**Calculus" Cengage Publications, 7thEd., 2019.

Web links and Video Lectures (e-Resources):

- http://nptel.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- VTU e-Shikshana Program
- VTU EDUSAT Program.

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

Digital System Design using Verilog		Semester	3
Course Code	**BEC302**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory/Practical		

Course objectives:

This course will enable students to:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
- Give Programming Assignments.

MODULE-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-McCluskey Minimization
Technique. Quine-McCluskey using Don't CareTerms.(Section3.1to3.5ofText1).

MODULE-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices(PLDs) (Section5.1to5.7 ofText2)

MODULE-3

Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops):SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.4, 6.6 to 6.9 (Excluding 6.9.3)of Text2)
MODULE-4
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section1.1to1.6.2, 1.6.4 (only Verilog),2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description.(Section2.1to2.2(only Verilog) of Text3)
MODULE-5
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (onlyVerilog)of Text 3) **Verilog Structural description**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section4.1 to 4.2 of Text 3)

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.N	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor(Full/half)circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type
8	To realize Counters-up/down (BCD and binary)using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops(SR, D,T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions

should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:
Books

1. Digital Logic Applications and Design by John MYarbrough,Thomson Learning,2001.
2. Digital Principles and Design by Donald DGivone,McGrawHill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress.

ReferenceBooks:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3. Fundamentals of HDL,by Cyril PR, Pearson/Sanguine2010

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
Programming Assignments/Mini Projects can be given to improve programming skills.

Electronic Principles and Circuits		Semester	3
Course Code	**BEC303**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory/Practical/Viva-Voce /Term-work/Others		

Course objectives:

This course will enable students to

- Design and analyse the BJT circuits as an amplifier and voltage regulation.
- Design of MOSFET Amplifiers and analyse the basic amplifier configurations using small signal equivalent circuit models
- Design of operational amplifiers circuits as Comparators, DAC and filters.
- Understand the concept of positive and negative feedback.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.
- Understand the thyristor operation and the different types of thyristors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

Transistor Biasing: Voltage Divider Bias, VDB Analysis, VDB Load line and Q point, Two supply Emitter Bias, Other types of Bias.

BJT AC models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters.

Voltage Amplifiers: Voltage gain, Loading effect of Input Impedance.

CC Amplifiers: CC Amplifier, Output Impedance.

[Text1]

MODULE-2

MOSFET

Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.

[Text 2]

MODULE-3
Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis. **Oscillator:** Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator. **The 555 timer**: Monostable Operation, Astable Operation. [Text1]
MODULE-4
Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation). **Active Filters:** Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters. [Text1]
MODULE-5
Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation. **Thyristors:** The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors. [Text1]

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.NO	Experiments
1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator
2	Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference.
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
5	Design and test Emitter Follower
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve.
8	Design and test Full wave Controlled rectifier using RC triggering circuit.
9	Design and test Precision Half wave and full wave rectifiers using Opamp
10	Design and test RC phase shift oscillator

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1

Web links and Video Lectures (e-Resources):

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Network Analysis		Semester	3
Course Code	**BEC304**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

1. Apply mesh and nodal techniques to solve an electrical network.
2. Solve different problems related to Electrical circuits using Network Theorems and Two port network.
3. Familiarize with the use of Laplace transforms to solve network problems.
4. Study two port network parameters and their applications.
5. Study of RLC Series and parallel tuned circuit.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative (Group)Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1

Basic Concepts: Practical sources, Source transformations, Network reduction using Star - Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.

Module-2

Network Theorems: Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.

Module-3

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and

RLC circuits for AC and DC excitations.

Module-4

Laplace Transformation &Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.

Module-5

Two port network parameters: Definition of Z,Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets.

Resonance:

Series Resonance: Variation of Current and Voltage with Frequency, SelectivityandBandwidth,Q-Factor,CircuitMagnificationFactor,Selectivity with Variable Capacitance, Selectivity with Variable Inductance.

Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, Land f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Determine currents and voltages using source transformation/ source shifting/ mesh/ nodal analysis and reduce given network using star- delta transformation.
2. Solve problems by applying Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.
3. Analyse the circuit parameters during switching transients and apply Laplace transform to solve the given network
4. Evaluate the frequency response for resonant circuits and the network parameters for two port networks

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. M.E.Van Valkenburg (2000), Network Analysis, Prentice Hall of India, 3rd edition, 2000, ISBN:9780136110958.
2. Roy Choudhury-Networks and Systems, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677

ReferenceBooks:

3. Hayt, Kemmerly and Durbin-Engineering Circuit Analysis, **TMH**7th Edition, 2010.
4. **J.**David Irwin/ R.Mark Nelms- Basic Engineering Circuit Analysis JohnWiley,8thed,2006.
5. Charles K Alexander and Mathew NO Sadiku-Fundamentals of Electric Circuits, Tata McGraw-Hill,3rc1 Ed,2009.

Web links and Video Lectures (e-Resources):
• .
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Analog and Digital Systems Design Laboratory		Semester	3
Course Code	**BECL305**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	Theory/Practical/Viva-Voce /Term-work/Others		

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.NO	**Experiments (***All the experiments has to be conducted using discrete components***)**
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192
	Demonstration Experiments (For CIE)
9	Design and Test the second order Active Filters and plot the frequency response, i) Low pass and Highpass Filter ii) Bandpass and Bandstop Filter
10	Design and test the following using 555 timer i) Monostable Multivibraator ii) Astable Multivibrator
11	Design and Test a Regulated Power supply
12	Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic circuit experiments using 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall

be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.
The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual", 5th Edition, 2009, Oxford University Press.
2. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

Electronic Devices		Semester	3
Course Code	**BEC306A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives: This course will enable students to:

- Understand the basics of semiconductor physics and electronic devices.
- Describe the mathematical models BJTs and FETs along with the constructional details.
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative(Group)Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the realworld-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1

Semiconductors

Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect.

(Text1:3.1.1,3.1.2,3.1.3,3.1.4,3.2.1,3.2.3,3.2.4,3.4.1,3.4.2,3.4.3,3.4.5).

Module-2

PN Junctions

Forward and Reverse biased junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers.**(Text1:5.3.1,5.3.3,5.4,5.4.1,5.4.2,5.4.3)** Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials.

(Text1:8.1.1,8.1.2,8.1.3,8.2,8.2.1),

Module-3

Bipolar Junction Transistor

Fundamentals of BJT operation, Amplification with BJTS,BJT Fabrication, The coupled Diode model(Ebers-Moll Model),Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

(Text1:7.1,7.2,7.3,7.5.1,7.6,7.7.1,7.7.2, 7.7.3)

Module-4

Field Effect Transistors

Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MO Sstructure-Energy band diagram, Ideal Capacitance

-Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics.

(Text2:9.1.1,9.4,9.6.1,9.6.2,9.7.1,9.7.2,9.8.1,9.8.2).

Module-5

Fabrication of p-n junctions

Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. **(Text 1: 5.1)**

Integrated Circuits

Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements.**(Text 1:9.1,9.2,9.3.1,9.3.3).**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the principles of semiconductor Physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of semiconductor junctions for circuits and systems.
5. Identify the mathematical models of MOS transistors for circuits and systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices",7th Edition,Pearson Education,2016,ISBN978-93-325-5508-2.
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition,McGraw **Hill** Education, 2012,ISBN 978-0-07- 107010-2.

ReferenceBooks:

3. S.M.Sze,KwokK.Ng,"PhysicsofSemiconductorDevices",3rd Edition, Wiley,2018.
4. AdirBar-Lev,"SemiconductorandElectronicDevices",3rd Edition,PHI, 1993

Web links and Video Lectures (e-Resources):

• .
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Sensors and Instrumentation		Semester	3
Course Code	**BEC306B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors
- Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operations of transducers and instrumentation amplifiers.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative(Group)Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the realworld-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1

Introduction to sensor based measurement systems:
General concepts and terminology, sensor classification, Primary Sensors, material for sensors, microsensor technology. (Text 1)

Module-2

Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors. (Text 1)

Module-3

Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error.(Text 2: 1.2-1.6)
Multirange Ammeters, Multirange voltmeter.(Text2:3.2,4.4)
Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM (Text 2: 5.1-5.3, 5.5,5.6)

Module-4

Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator.
Bridges: Measurement of resistance: Wheatstone's Bridge, AC Bridges - Capacitance and Inductance Comparison bridge, Wien's bridge.

(Text2:refer 6.2,6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8, 11.2, 11.8 -11.10, 11.14).

Module-5

Transducers: Introduction,ElectricalTransducer,ResistiveTransducer,Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT.
(Text2:13.1-13.3,13.5, 13.6 up to 13.6.1,13.7,13.8,13.11).
Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale(Text2:14.3.3, 14.4.1, 14.4.3).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the material properties required to make sensors
2. Understand the principle of transducers for measuring physical parameters.
3. Describe the manufacturing process of sensors
4. Analyze the instrument characteristics and errors.
5. Describe the principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. "Sensors and Signal Conditioning", Ramon Pallas Areny, JohnG. Webster,2nd edition, John Wiley and Sons,2000
2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill,3rdEdition,2012,ISBN:9780070702066.

Reference Books

1. DavidA. Bell,"Electronic Instrumentation & Measurements", Oxford University Press PHI 2ndEdition, 2006,ISBN 81-203-2360-2.
2. D. HelfrickandW.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1stEdition, 2015, ISBN: 9789332556065.

Web links and Video Lectures (e-Resources):

• .
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Computer Organization and Architecture		Semester	3
Course Code	**BEC306C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives: This course will enable students to:

- Explain the basic sub systems of a computer, their organization, structure and operation.
- Illustrate the concept of programs as sequences of machine instructions.
- Demonstrate different ways of communicating with I/O devices
- Describe memory hierarchy and concept of virtual memory.
- Illustrate organization of simple pipelined processor and other computing systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance -Processor Clock, Basic Performance Equation(**upto1.6.2ofChap1ofText).**

Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**

Module-2

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions **(from2.4.7ofChap2, except 2.9.3, 2.11 & 2.12 of Text).**

Module-3

Input/ Output Organization: Accessing I/O Devices, Interrupts -Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access (upto4.2.4and4.4except4.4.1ofChap4ofText).

Module-4

Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage- Magnetic Hard Disks **(5.1,5.2,5.2.1,5.2.2,5.2.3,5.3,5.5(except 5.5.1 to** 5.5.4), 5.7 (except5.7.1), 5.9, 5.9.1 of Chap 5 of Text).

Module-5

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control **(up to 7.5 except 7.5.1 to7.5.6 of Chap 7 of Text).**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basic organization of a computer system.
2. Describe the addressing modes, instruction formats and program control statement.
3. Explain different ways of accessing an input/ output device including interrupts.
4. Illustrate the organization of different types of semiconductor and other secondary storage memories.
5. Illustrate simple processor organization based on hard wired control and micro-programmed control.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Book

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition,Tata McGrawHill,2002.

ReferenceBooks:

2. David A. Patterson, John L. Hennessy: Computer Organization and Design-The Hardware/ Software InterfaceARM Edition, 4th Edition, Elsevier,2009.
3. William Stallings: Computer Organization &Architecture,7th Edition, PHI, 2006.
4. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

Web links and Video Lectures (e-Resources):
• .
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
•

Applied Numerical Methods for EC Engineers		Semester	3
Course Code	**BEC306D**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	**Theory**		

Course objectives:

- To provide the knowledge and importance of error analysis in engineering problems
- To represent and solve an application problem using a system of linear equations
- Analyzeregression **data** to choose the most appropriate model for a situation.
- Familiarize with the ways of solving complicated mathematical problems numerically
- Prepare **to solve** mathematical models represented by initial or boundary value problems

Teaching-Learning Process

Pedagogy (General Instructions):

These are sample Strategies, teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

Module-1: Errors in computations and Root of the equations

Approximations and Round Off -Errors in computation: Error definitions, Round-Offerrors, Truncation errors and the Taylor series-The Taylor series, Error Propagation, Total numerical error,Absolute,Relative and percentage errors,Blunders, Formulation errors and data uncertainty. Roots of equations: Simple fixed point iteration methods. Secant Method, Muller's method, and Graeffe's Roots Squaring Method. Aitkin's Method. **(8 hours)**

(RBT Levels: L1, L2 and L3)

Module-2: Solution of System of Linear Equations

Rank of the matrix, Echelon form, Linearly dependent and independent equations, Solutions for linear equations, Partition method, Croute's Triangularisation method. Relaxation method. Solution of non-linear simultaneous equations by Newton-Raphson method. Eigen Values and properties, Eigen Vectors, Bounds on Eigen Values, Jacobi's method, Given's method for symmetric matrices. **(8 hours)**

(RBT Levels: L1, L2 L3)

Module-3: Curve Fitting
Least-Squares Regression: Linear Regressions, Polynomial regressions, Multiple Linear regressions, General Linear Least squares, Nonlinear Regressions, QR Factorization. Curve Fitting with Sinusoidal Functions Introduction to Splines,Linear Splines, Quadratic Splines, Cubic Splines. Bilinear Interpolation. **(8 hours)** **(RBT Levels: L1, L2 L3)**
Module-4: Numerical integration, Difference equations and Boundary Value Problems
Romberg's method, Euler-Maclaurin formula, Gaussian integration for n = 2 and n=3. Numerical double integration by trapezoidal and Simpson's 1/3 rd rule. Solution of linear difference equations. Boundary-Value Problems, Introduction. The Shooting Method, Finite-Difference Methods **(8 hours)** **(RBT Levels: L1, L2 and L3)**
Module-5: Numerical solution of partial differential equations
Classifications of second-order partial differential equations,Finite difference approximations to partial derivatives. Solution of:Laplace equation, Poisson equations, one-dimensional heat equation and wave equations. **(8 hours)** **(RBT Levels: L1, L2 and L3)**
Course outcome (Course Skill Set) At the end of the course, the student will be able to: 1. Explain and measure errors in numerical computations 2. Test for consistency and solve a system of linear equations. 3. Construct a function which closely fits given n- n-points of an unknown function. 4. Understand and apply the basic concepts related to solving problems by numericaldifferentiation and numerical integration. 5. Use appropriate numerical methods to study phenomena modelled as partial differential equations.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE, the minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the **CIE** (Continuous Internal Evaluation) and **SEE** (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)

Text Books:

1. **Steven C. Chapra & Raymond P. Canale: "**Numerical Methods for Engineers and Scientists", McGraw Hill, 8th Edition, 2020.
2. **Steven C. Chapra**: "Applied Numerical Methods with MATLAB for Engineers and Scientists", McGraw Hill, Fifth Edition, 2023.
3. **B. S. Grewal**: "Numerical Methods in Engineering & Science with programs in C, C++ and MATLAB", Khanna Publishers, 10hEd., 2015.

Reference Books:

1. **John H. Mathews & Kurtis D. Frank**: "Numerical Methods Using MATLAB", PHI Publications, 4th Edition, 2005.
2. **Won Young Yang, Wenwu Cao, Tae Sang Chung, John Morris: "**Applied Numerical Methods Using MATLAB**",** WILEY Interscience**,** Latest Edition, 2005.

Web links and Video Lectures (e-Resources):

- http://nptel.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- VTU e-Shikshana Program
- VTU EDUSAT Program.

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

Lab VIEW Programming		Semester	3
Course Code	**BEC358A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Total	100
		Exam Hours	2
Examination type (SEE)	Practical		

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various tool bars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.

Sl.NO	VI Programs(using LabVIEW software)to realize the following:
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of ‘n’ numbers using ‘for’ loop
4	Factorial of a given number using ‘for’ loop
5	Determine square of a given number
6	Factorial of a given number using ‘while‘ loop
7	Sorting even numbers using ‘while’ loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	DemonstratehowtocreateabasicVIwhichcalculatestheareaandperimeterofacircle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Use LabVIEW to create data acquisition, analysis and display operations
- Create user interfaces with charts, graph and buttons
- Use the programming structures and data types that exist in LabVIEW
- Use various editing and debugging techniques.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. VirtualInstrumentationusingLABVIEW,JovithaJerome,PHI,2011
2. VirtualInstrumentationusingLABVIEW,SanjayGupta,JosephJohn,TMH,McGrawHill,SecondEdition,2011.

MATLAB Programming		Semester	3
Course Code	**BEC358B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0	SEE Marks	50
Total Hours of Pedagogy	14	Total Marks	100
Credits	01	Exam Hours	1
Examination type (SEE)	Theory		

Course objectives:

- Understand the MATLAB commands and functions.
- Create and Execute the script and function files
- Work with built in function, saving and loading data and create plots.
- Work with the arrays, matrices, symbolic computations, files and directories.
- Learn MATLAB programming with script, functions and language specific features.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Adopt Problem Based Learning (PBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
2. Give programming assignments.

Module-1

Introduction: Basics of MATLAB, Simple arithmetic calculations, Creating and working with arrays and numbers.

Module-2

Creating and printing simple plots, Creating, saving and executing a script file, Creating and executing a function file, Working with arrays and matrices.

Module-3

Working with anonymous functions, Symbolic Computations, Importing and exporting data, Working with files and directories.

Module-4

Interactive computations: Matrices and vectors, Matrix and array operations, Character strings, Command line functions, Built-in functions, Saving and loading data, Plotting simple plots.

Module-5

Programming in MATLAB: Script Files, Function Files, Language specific Features.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the syntax of MATLAB for arithmetic computations, arrays, matrices.
2. Understand the built in function, saving and loading data, and create plots
3. Create program using symbolic computations, Importing and exporting data and files
4. Create program using character strings, Command line functions and Built-in functions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

1. The question paper will have ten questions. Each question is set for 10 marks.
2. There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
3. The students have to answer 5 full questions, selecting one full question from each module.
4. **The duration of the examinations shall be defined by the concerned board of studies**

Suggested Learning Resources:

Book

1. Rudra Pratap, Getting Started with MATLAB – A quick Introduction for scientists and Engineers, Oxford University Press, 2010.

Web links and Video Lectures (e-Resources):

- .

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

-

C++ Basics		Semester	4
Course Code	**BEC358C**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Total Hours of Pedagogy	24	Total Marks	100
Credits	1	Exam Hours	02
Examination nature (SEE)	Practical		

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	Experiments
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.
11	Write a C++ program to create three objects for a class named count object with data members

	such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and

result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

IoT for Smart Infrastructure		Semester	3
Course Code	**BEC358D**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	14	Total Marks	100
Credits	01	Exam Hours	1
Examination type (SEE)	Theory/Practical		

Course objectives:

- To provide an understanding of the concepts, principles, and applications of IoT in the context of smart infrastructure.
- To explore the role of IoT technologies in transforming infrastructure into smart, efficient, and sustainable systems and analyse the challenges, opportunities, and considerations in implementing IoT for smart infrastructure.
- To examine real-world case studies and successful implementations of IoT in smart cities, buildings, transportation, and energy management and explore future trends and emerging technologies shaping the field of IoT for smart infrastructure.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- **Interactive Lectures:** Conduct interactive lectures to present the theoretical concepts and foundational knowledge of IoT for smart infrastructure.
- **Case Studies and Group Discussions:** Utilize case studies to analyse real-world implementations of IoT in smart infrastructure projects. Divide students into groups and assign them specific cases to discuss and analyse.
- **Hands-on Workshops and Simulations:** Organize hands-on workshops or simulations where students can interact with IoT devices and technologies relevant to smart infrastructure.
- **Guest Lectures and Industry Experts:** Invite guest speakers or industry experts who have hands-on experience in implementing IoT in smart infrastructure projects. They can share their insights, challenges, and success stories, providing students with a real-world perspective
- **Project-Based Learning:** Assign students to work on individual or group projects related to IoT for smart infrastructure. Provide a project brief with specific objectives and deliverables. Students can apply their knowledge and skills to design, develop, or analyse IoT solutions for smart infrastructure challenges.

Module-1

Introduction to IoT and Smart Infrastructure

Introduction to IoT: Definition of IoT and its basic components, Overview of IoT applications in various industries, Importance of IoT in transforming infrastructure.

Smart Infrastructure Overview: Introduction to smart infrastructure and its key components, Benefits and challenges of implementing smart infrastructure, Case studies showcasing successful smart infrastructure projects.

IoT Technologies for Smart Infrastructure: Sensors and actuators: Types, functionalities, and applications; Communication protocols: Wi-Fi, Bluetooth, cellular networks, and their use in IoT;

Cloud computing and data analytics in IoT for infrastructure; Edge computing: Real-time decision-making at the edge.
Security and Privacy in IoT for Smart Infrastructure: Security challenges and threats in IoT,Privacy considerations and data protection in smart infrastructure, best practices and solutions for ensuring IoT security and privacy.

Module-2

IoT Applications in Smart Cities

Introduction to Smart Cities - Definition and key features of smart cities, Role of IoT in transforming cities into smart cities, Benefits and challenges of smart city implementations.
IoT Applications in Smart City Infrastructure - Smart transportation: Intelligent traffic management and transportation systems, Smart buildings: Energy management and occupant comfort; Smart grids: Optimizing energy distribution and consumption; Waste management, water management, and environmental monitoring.
Case Studies of Smart City Implementations: Showcase of successful smart city projects around the world; Analysis of the IoT technologies and strategies implemented; Lessons learned from these case studies.
Future Trends in Smart Cities: Emerging technologies shaping the future of smart cities, Role of IoT, AI, and 5G in advancing smart city infrastructure, Opportunities and challenges for future smart city developments.

Module-3

IoT Applications in Smart Buildings

Introduction to Smart Buildings: Definition and key features of smart buildings, Benefits of IoT in improving energy efficiency and occupant comfort, Challenges and considerations in implementing smart building technologies.
IoT Technologies for Smart Buildings: Building automation systems and controls; Energy management and monitoring using IoT devices; Indoor environmental quality monitoring and optimization; Smart lighting and HVAC systems.
Case Studies of Smart Building Implementations: Showcase of successful smart building projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies.
Future Trends in Smart Buildings: Emerging technologies for smart buildings; Integration of IoT with AI and machine learning; Potential impact of 5G on smart building applications.

Module-4

IoT Applications in Smart Transportation

Introduction to Smart Transportation: Definition and key features of smart transportation; Role of IoT in intelligent traffic management and transportation systems; Challenges and opportunities in implementing smart transportation solutions.
IoT Technologies for Smart Transportation: Traffic sensors and monitoring systems; Intelligent transportation systems (ITS); Vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communication; Real-time data analysis and predictive analytics.

Case Studies of Smart Transportation Implementations: Showcase of successful smart transportation projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies.

Future Trends in Smart Transportation: Emerging technologies shaping the future of smart transportation; Role of IoT, AI, and autonomous vehicles; Potential impact of 5G on smart transportation applications.

Module-5

IoT for Smart Grids and Energy Management

Introduction to Smart Grids: Definition and key features of smart grids: Role of IoT in optimizing energy distribution and consumption; Benefits and challenges of smart grid implementations. IoT Technologies for Smart Grids: Smart meters and energy monitoring devices; Demandresponse and load management; Grid optimization and fault detection using IoT; Renewableenergy integration and grid stability.

Case Studies of Smart Grid Implementations: Showcase of successful smart grid projects, Analysis of IoT technologies and solutions deployed, Lessons learned from these case studies.

Future Trends in Smart Grids and Energy Management: Emerging technologies for smart grids; Integration of IoT, AI, and blockchain in energy management; Potential impact of 5G on smart grid applications.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

- Define and explain the core concepts and components of IoT and its relevance to smart infrastructure. Identify and evaluate the key technologies and communication protocols used in IoT for smart infrastructure.
- Assess the benefits, challenges, and ethical considerations associated with implementing IoT in smart infrastructure projects and analyse & compare different IoT applications in smart cities, buildings, transportation, and energy management.
- Examine real-world case studies of successful IoT implementations in smart infrastructure and extract lessons learned. Demonstrate an understanding of security and privacy considerations in IoT for smart infrastructure.
- Discuss the impact of emerging technologies, such as artificial intelligence and 5G, on the future of IoT in smart infrastructure. Apply knowledge and critical thinking skills to propose IoT-based solutions for smart infrastructure challenges.
- Work effectively in teams to analyse, design, and present IoT projects related to smart infrastructure and communicate effectively and articulate the potential benefits and limitations of IoT for smart infrastructure.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's
taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to securea minimum of 35% of the maximum marks meant for SEE.

~~OR~~

~~MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then~~

1. ~~The question paper will have ten questions. Each question is set for 10 marks.~~
2. ~~There will be 2 questions from each module. Each of the two questions under a module may or may not have the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).~~
3. ~~The students have to answer 5 full questions, selecting one full question from each module.~~

Suggested Learning Resources:

1. MindMatrix.io
2. "Internet of Things (A Hands-on-Approach)" by Arshdeep Bahga and Vijay Madisetti
3. "Building the Internet of Things: Implement New Business Models, Disrupt Competitors, Transform Your Industry" by Maciej Kranz
4. "Smart Cities: Big Data, Civic Hackers, and the Quest for a New Utopia" by Anthony M.
   Townsend

5. "Internet of Things for Architects: Architecting IoT solutions by implementing sensors, communication infrastructure, edge computing, analytics, and security" by Perry Lea.

Web links and Video Lectures (e-Resources):

- makes.mindmatrix.io

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Sensor Deployment and Data Collection: Organize a hands-on activity where participants work in groups to deploy sensors in a simulated smart infrastructure environment.
- Smart City Simulation Game: Develop a simulation game where participants take on different roles representing stakeholders in a smart city.
- IoT Solution Design Challenge: Assign participants to design an IoT-based solution for a specific smart infrastructure problem. They can work individually or in teams to identify the problem, propose an IoT solution, outline the required components and technologies, and create a prototype or presentation.
- Security and Privacy Risk Assessment: Conduct a group activity where participants analyse the security and privacy risks associated with IoT deployments in smart infrastructure.
- Field Visit to Smart Infrastructure Project: Organize a field visit to a smart infrastructure project, such as a smart building, smart city district, or IoT-enabled transportation system.

ELECTROMAGNETIC THEORY		Semester	IV
Course Code	**BEC401**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

Thiscoursewillenablestudentsto:

- Study the different coordinate systems, Physical significance of Divergence, Curl andGradient.
- UnderstandtheapplicationsofCoulomb'slawandGausslawtodifferentchargedistributionsand the applications of Laplace's and Poisson's Equations to solve real time problems oncapacitanceofdifferent chargedistributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theoremfordifferent current distributions.
- Infertheeffectsofmagneticforces,materialsandinductance.
- KnowthephysicalinterpretationofMaxwell'sequationsandapplicationsforPlanewavesforthe irbehavior in different media.
- AcquireknowledgeofPoyntingtheorem anditsapplicationofpower flow

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

ThesearesampleStrategies,whichteacherscanusetoacceleratetheattainmentofthevariouscourseoutcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various courseoutcomes.

1. Lecturemethod (L)doesnot meanonlytraditionallecturemethod,butdifferenttypesofteachingmethodsmaybe adopted todeveloptheoutcomes.
2. Encouragecollaborative (Group) Learningintheclass.
3. AskatleastthreeHOTS (HigherOrderThinking) questionsintheclass,whichpromotescriticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuchastheabilityto evaluate,generalize,and analyzeinformationratherthansimplyrecallit.
5. Topicswillbeintroducedinamultiplerepresentation.
6. Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeupwithcreati ve ways to solvethem.
7. Discusshoweveryconceptcanbeappliedtothereal world andwhenthat'spossible,ithelpsimprovethe student'sunderstanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussionson thetopicinthesucceedingclasses.

Module-1

Revision of Vector Calculus – (**Text 1: Chapter 1**)

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. (**Text: Chapter 2.1 to 2.5, 3.1**) **RBT Level:** L1, L2, L3

Module-2

Gauss's Law and Divergence: Gauss 'law, Application of Gauss' law to Point Charge, line charge, Surface charge and Volume Charge, Point (differential) form of Gauss law, Divergence. Maxwell's First Equation (Electrostatics), Vector Operator ▼and divergence theorem, Numerical Problems (**Text: Chapter 3.2 to 3.7).**Energy expended or work done in moving a point charge in anElectric field, The line integral (**(Text: Chapter 4.1 and 4.2**) Current and Current density, Continuity of current. (**Text: Chapter 5.1, 5.2**) **RBT Level:** L1, L2, L3

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Examples of the solution of Laplace's equation, Numerical problems on Laplace's equation
(**Text: Chapters 7.1 and 7.3**)
Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density.
(**Text: Chapters 8.1 to 8.5**) **RBT Level:** L1, L2, L3

Module-4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).**
Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, the magnetic circuit, problems (**Text: Chapter 9.6 to 9.8**) **RBT Level:** L1, L2, L3

Module-5

Faraday's law of Electromagnetic Induction –Integral form and Point form, Numerical problems. Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems (**Text: Chapter10.1 to10.4**)
Uniform Plane Wave: Wave propagation in free space, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations,Poynting's Theorem and wave power, Skin effect or Depth of penetration, Numerical problems. (**Text: Chapter 12.1, 12.3, 12.4**) **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.
3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Book:

1. W.H. Hayt and J.A. Buck, —Engineering Electromagnetics, 8th Edition, Tata McGraw- Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford University press, 4thEdn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balman, PHI, 2ndEdn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. N. Narayana Rao, —Fundamentals of Electromagnetics for Engineering, Pearson

Web links and Video Lectures (e-Resources):

- NPTEL Video lectures : https://youtu.be/pGdr9WLto4A
- NPTEL Video lectures: https://youtu.be/xn2IpxI991M

ActivityBasedLearning(SuggestedActivitiesinClass)/Practical-Based Learning

- Group Discussion/Quiz
- Demonstration of Electromagnetic concepts.
- Case Study on Medical Imaging devices.

PRINCIPLES OF COMMUNICATION SYSTEMS		Semester	4
Course Code	**BEC402**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory/practical/Viva-Voce /Term-work/Others		

Course objectives:

This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM
- Design and analyse the electronic circuits for AM and FM modulation and demodulation.
- Understand the concepts of random variable and random process to model communication systems.
- Understand and analyse the concepts of digitization of signals.
- Evolve the concept of SNR in the presence of channel induced noise

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

Random Variables and Processes: Introduction, Probability, Conditional Probability, Random variables. Statistical Averages: Function of a random variable, Moments, Random Processes, Mean, Correlation and Covariance function: Properties of autocorrelation function, Cross–correlation functions, Gaussian Process: Gaussian Distribution Function.

[Text 2: 5.1, 5.2,5.3,5.4,5.5,5.6,5.9]

RBT: L1, L2

MODULE-2

Amplitude Modulation Fundamentals: AM Concepts, Modulation index and Percentage of Modulation, Sidebands and the frequency domain, AM Power, Single Sideband Modulation.

AM Circuits: Amplitude Modulators: Diode Modulator, Transistor Modulator, collector Modulator. Amplitude Demodulators: Diode Detector, Balanced Modulators: Lattice Modulators.

Frequency Division Multiplexing: Transmitter-Multiplexer, Receiver-Demultiplexer.

[Text1: 3.1, 3.2,3.3,3.4,3.5,4.2,4.3,4.4,10.2]

RBT: L1, L2, L3

MODULE-3

Fundamentals of Frequency Modulation: Basic Principles of Frequency Modulation, Principles of Phase Modulation, Modulation index and sidebands, Noise Suppression Effects of FM, Frequency Modulation versus Amplitude Modulation.

FM Circuits: Frequency Modulators: Voltage Controlled Oscillators. , Frequency Demodulators: Slope Detectors, Phase Locked Loops.

Communication Receiver: Super heterodyne receiver, Frequency Conversion: Mixing Principles, JFET Mixer.

[Text1: 5.1,5.2,5.3,5.4,5.5,6.1,6.3,9.2,9.3]

RBT: L1, L2, L3

MODULE-4
Digital Representation of Analog Signals: Introduction, Why Digitize Analog Sources?, The Sampling process, Pulse Amplitude Modulation, Time-Division Multiplexing, Pulse Position Modulation: Generation and Detection of PPM wave. The Quantization Process. Pulse Code Modulation: Sampling, Quantization, Encoding, line Codes, Differential encoding, Regeneration, Decoding, filtering, multiplexing. **[Text2: 7.1,7.2,7.3,7.4,7.5,7.6,7.8,7.9]** **RBT: L1,L2,L3**
MODULE-5
Baseband Transmission of Digital signals: Introduction, Intersymbol Interference, Eye Pattern, Nyquist criterion for distortionless Transmission, Baseband M-ary PAM Transmission. **[Text2:8.1,8.4,8.5,8.6,8.7]** **Noise:** Signal to Noise Ratio, External Noise, Internal Noise, Semiconductor Noise, Expressing Noise Levels, Noise in Cascade Stages. **[Text1:9.5]** **RBT:L1,L2,L3**

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted using MATLAB/SCILAB/OCTAVE)*

Sl.NO	Experiments
1	Basic Signals and Signal Graphing: a) unit Step, b) Rectangular, c) standard triangle d) sinusoidal and e) Exponential signal.
2	Illustration of signal representation in time and frequency domains for a rectangular pulse.
3	Amplitude Modulation and demodulation: Generation and display the relevant signals and its spectrums.
4	Frequency Modulation and demodulation: Generation and display the relevant signals and its spectrums.
5	Sampling and reconstruction of low pass signals. Display the signals and its spectrum.
6	Time Division Multiplexing and demultiplexing.
7	PCM Illustration: Sampling, Quantization and Encoding
8	Generate a)NRZ, RZ and Raised cosine pulse, b) Generate and plot eye diagram
9	Generate the Probability density function of Gaussian distribution function.
10	Display the signal and its spectrum of an audio signal.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the principles of analog communication systems and noise modelling.
2. Identify the schemes for analog modulation and demodulation and compare their performance.
3. Design of PCM systems through the processes sampling, quantization and encoding.
4. Describe the ideal condition, practical considerations of the signal representation for baseband transmission of digital signals.
5. Identify and associate the random variables and random process in Communication system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.
2. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.

Reference Books

1. B P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1

Web links and Video Lectures (e-Resources):

1. Principles of Communication Systems **https://nptel.ac.in/courses/108104091**
2. Communication Engineering **https://nptel.ac.in/courses/117102059**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Assignments and test – Knowledge level, Understand Level and Apply level
2. Experiential Learning by using free and open source software's SCILAB or OCTAVE
3. Open ended questions by faculty, Open ended questions from students

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication EngineeringNEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2023 – 24)

IV Semester

Control Systems			
Course Code	**BEC403**	CIE Marks	50
Teaching Hours/Week (L: T: P)	(3:0:2)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
2. Understand Time domain and Frequency domain analysis.
3. Analyze the stability of a system from the transfer function
4. Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up withtheir own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and havediscussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical Systems, Electrical Systems, Analogous Systems. (Textbook 1: Chapter 1.1, 2.2)

Teaching-LearningProcess	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2	
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs. (Textbook 1: Chapter 2.4, 2.5, 2.6)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to implement block diagram reduction techniques and Signal Flow graphs **RBT Level:** L1, L2, L3
Module-3	
Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design). (Textbook 1: Chapter 5.3, 5.4, 5.5)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to show time response for various transfer functions and PI, PD and PID controllers. **RBT Level:** L1, L2, L3
Module-4	
Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion. **Introduction to Root-Locus Techniques**, The root locus concepts, Construction of root loci. (Textbook 1: Chapter 6.1, 6.2, 6.4, 6.5, 7.1, 7.2, 7.3)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to plot Root locus for various transfer functions **RBT Level:** L1, L2, L3
Module-5	
Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. (Textbook 1: Chapter 4: 8.1, 8.2, 8.4) Mathematical preliminaries, Nyquist Stability criterion, (Stability criteria related to polar plots are excluded) (Textbook 1: 9.2, 9.3) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 1: 12.2, 12.3, 12.6)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to draw Bode plot for various transfer functions **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software (P-Spice/ MATLAB / Python / Scilab / OCTAVE / LabVIEW) demonstrate the operation of the following circuits:

Sl.No	Experiments
1	Implement Block diagram reduction technique to obtain transfer function a control system.
2	Implement Signal Flow graph to obtain transfer function a control system.
3	Simulation of poles and zeros of a transfer function.
4	Implement time response specification of a second order Under damped System, for different damping factors.
5	Implement frequency response of a second order System.
6	Implement frequency response of a lead lag compensator.
7	Analyze the stability of the given system using Routh stability criterion.
8	Analyze the stability of the given system using Root locus.
9	Analyze the stability of the given system using Bode plots.
10	Analyze the stability of the given system using Nyquist plot.
11	Obtain the time response from state model of a system.
12	Implement PI and PD Controllers.
13	Implement a PID Controller and hence realize an Error Detector.
14	Demonstrate the effect of PI, PD and PID controller on the system response.

Course Outcomes

At the end of the course the student will be able to:

1. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
2. Calculate time response specifications and analyse the stability of the system.
3. Draw and analyse the effect of gain on system behaviour using root loci.
4. Perform frequency response Analysis and find the stability of the system.
5. Represent State model of the system and find the time response of the system.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5^{th} week of the semester
- Second test at the end of the 10^{th} week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4^{th} week of the semester
- Second assignment at the end of 9^{th} week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15^{th} week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify inthe SEE. Marks secured out of 100 shall be reduced proportionally to 50.

Suggested Learning Resources:

Text Books

1. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

Communication Laboratory		Semester	4
Course Code	**BECL404**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	03
Examination type (SEE)	Theory/Practical/Viva-Voce /Term-work/Others		

Course objectives:

This laboratory course enables students to

- Understand the basic concepts of AM and FM modulation and demodulation.
- Design and analyse the electronic circuits used for AM and FM modulation and demodulation circuits.
- Understand the sampling theory and design circuits which enable sampling and reconstruction of analog signals.
- Design electronic circuits to perform pulse amplitude modulation, pulse position modulation and pulse width modulation.

	Experiments (Experiments to be conducted using hardware components)
1	Design and test a high-level collector Modulator circuit and Demodulation the signal using diode detector.
2	Test the Balanced Modulator / Lattice Modulator (Diode ring)
3	Design a Frequency modulator using VCO and FM demodulator using PLL (Use IC566 and IC565).
4	Design and plot the frequency response of Preemphesis and Deemphasis Circuits
5	Design and test BJT/FET Mixer
6	Design and test Pulse sampling, flat top sampling and reconstruction
7	Design and test Pulse amplitude modulation and demodulation.
8	Generation and Detection of Pulse position Modulation
9	Generation and Detection of Pulse Width Modulation
10	PLL Frequency Synthesizer
11	Data formatting and Line Code Generation
12	PCM Multiplexer and Demultiplexer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Illustrate the AM generation and detection using suitable electronic circuits.
2. Design of FM circuits for modulation, demodulation and noise suppression.
3. Design and test the sampling, Multiplexing and pulse modulation techniques using electronic hardware.
4. Design and Demonstrate the electronic circuits used for RF transmitters and receivers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.

MICROCONTROLLERS		Semester	4
Course Code	**BEC405A**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type(SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the difference between Microprocessor and Microcontroller and embedded microcontrollers.
- Analyze the basic architecture of 8051microcontroller.
- Program 8051 microcontroller using Assembly Language and C.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051
- Understand the interrupt structure of 8051 and Interfacing I/O devices using I/O ports of 8051.

Teaching-Learning Process(General Instructions)

The samples strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative(Group)Learning in the class
4. Ask at least three HOTS(Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical kills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the students' understanding.
   Give Programming Assignments.

	RBT Level
Module-1 (8 Hrs)	
Microcontroller: Microprocessor Vs Microcontroller, Micro controller & Embedded Processors, Processor Architectures-Harvard Vs Princeton & RISC Vs CISC , 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. (Text book 1-1.1,Text book 2-1.0,1.1,3.0,3.1,3.2,3.3 Text book 3-Pg 5-9)	**L1,L2**
Module-2 (8 Hrs)	
Instruction Set: 8051 Addressing Modes, Data Transfer Instructions, Arithmetic instructions, Logical Instructions, Jump & Call Instructions Stack & Subroutine Instructions of 8051 (with examples in assembly Language). (Text book 2- Chapter 5,6,7,8, **Additional reading Refer Textbook 3, Chapter 3 for complete understanding of instructions with flow diagrams)**	**L1,L2**

Module-3 (8 Hrs)	
Timers/Counters & Serial port programming: Basics of Timers & Counters, Data types & Time delay in the 8051 using C, Programming 8051 Timers, Mode 1 & Mode 2 Programming, Counter Programming (Assembly Language only). (Text book 2- 3.4, Text book 1- 7.1, 9.1,9.2) Basics of Serial Communication, 8051 Connection to RS232, Programming the 8051 to transfer data serially & to receive data serially using C.(Text book 2- 3.5, Text book 1- 10.1,10.2,10.3 except assembly language programs, 10.5)	**L1,L2, L3**
Module-4 (8 Hrs)	
Interrupt Programming: Basics of Interrupts, 8051 Interrupts, Programming Timer Interrupts, Programming Serial Communication Interrupts, Interrupt Priority in 8051(Assembly Language only) (Text book 2- 3.6, Text book 1- 11.1,11.2,11.4, 11.5)	**L1,L2, L3**
Module-5 (8 Hrs)	
I/O Port Interfacing & Programming: I/O Programming in 8051 C, LCD interfacing, DAC 0808 Interfacing, ADC 0804 interfacing, Stepper motor interfacing, DC motor control & Pulse Width Modulation (PWM) using C only. (Text book 1- 7.2, 12.1, 13.1, 13.2, 17.2, 17.3)	**L1, L2, L3**

Course outcome (Course Skill Set)

At the end of the course, students will be able to:

1. Describe the difference between Microprocessor and Microcontroller, Types of Processor Architectures and Architecture of 8051Microcontroller.
2. Discuss the types of 8051 Microcontroller Addressing modes & Instructions with Assembly Language Programs.
3. Explain the programming operation of Timers/Counters and Serial port of 8051 Microcontroller.
4. Illustrate the Interrupt Structure of 8051 Microcontroller & its programming.
5. Develop C programs to interface I/O devices with 8051 Microcontroller.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is 50%.The minimum passing mark for the CIE is 40%of the maximum marks(20marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to50 marks

Suggested Learning Resources:

TEXT BOOKS

1. The "8051 Microcontroller and Embedded Systems – Using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollind. Mckinlay; Phi, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth j. Ayala, 3rd edition, Thomson/Cengage Learning.
3. "Programming And Customizing The 8051 Microcontroller".,Myke Predko Tata Mc Graw-Hill Edition 1999 (reprint 2003).

REFERENCEBOOKS:

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web links and Video Lectures(e-Resources):

https://youtu.be/pA6K5NgWTow?si=zQqqgXQq50dVL_-s

Industrial Electronics		Semester	IV
Course Code	**BEC405B**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives: This course will enable student to

- Explain broad types of industrial power devices, there structure, and its characteristics.
- Design and analyse the broad categories of power electronic circuits.
- Explain various types of MEMs devices, principle of operation and construction.
- Familiarize with soft core processors and computer architecture.
- Apply protective methods for devices and circuits.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Industrial Power Devices: General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes **(Text book 1: 2.5, 2.6)**, Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs **(Text book 1: 4.3, 4.4, 4.6, 4.7**

Module-2

Power Electronics Circuits:), Thyristor, Thyristor characteristics, two transistor model **(Text book 1: 9.2, 9.3, 9.4)**.Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load **(Text book 1: 10.2, 10.3, 10.4)**.

Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators **(Text book 1: 5.9.1, 5.9.2, 5.9.3, 5.10)**

Module-3

Inverters – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter **(Text book 1: 6.3, 6.4, 6.5, 6.9)**.

AC voltage controllers – Single phase full wave controller with resistive load, single phase full wave controller with inductive load **(Text book 1: 11.3, 11.4)**.

Module-4

MEMS Devices: Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. **(Text book 2: 13.1, 13.3, 13.4)**

MEMS Applications: Introduction, Industrial, Automotive, Biomedical (**Text book 2:15.1, 15.2, 15.3, 15.4)**

Module-5

Protections of Devices and Circuits: Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Voltage protection by Selenium Diodes and Metaloxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards **(Text book 1: 17.2, 17.3, 17.4, 17.5, 17.6, 17.7, 17.8, 17.9)**.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, there structure, and its operating characteristics.
2. Design and analyse the power electronic circuits such as switch mode regulators, inverters, controlled rectifiers and ac voltage controllers.
3. Explain various types of MEMs devices used for sensing pressure, temperature, current, voltage, humidity, vibration etc..
4. Familiarize with soft core processors such as ASIC and FPGA.
5. Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
6. Apply protective methods for devices various industrial power devices based on thermal requirements and develop protective methods for the circuits against various electrical parameters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2. Fundamentals of Industrial Electronics , Bogdan M. Wilamowski, J. David Irwin, CRC Press, 2011,

Reference Books

1. Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
2. Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd, 2008.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/108/102/108102145/
- https://nptel.ac.in/courses/117105082
- https://www.youtube.com/channel/UCKg8GNii0Q-ieXE56AXosGg/featured
- https://www.ieee-ies.org/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz and Seminars

OPERATING SYSTEM		Semester	4
Course Code	**BEC405C**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type(SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management. Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Teaching-Learning Process(General Instructions)

The samples strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

	RBT Level
Module-1	
Introduction to Operating Systems: OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems **(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).**	**L1,L2**
Module-2	
Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux **(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).**	**L1,L2, L3**

Module-3	
Memory Management: Contiguous Memory allocation, Non-Contiguous Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux **(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text)**	**L1,L2, L3**
Module-4	
File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access **(Topics from Sections 7.1 to 7.8 of Text).**	**L1,L2**
Module5	
Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention **(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).**	**L1, L2**

Course outcome (Course Skill Set)

At the end of the course, students will be able to:

1. Explain the goals, structure, operation and types of operating systems.
2. Apply scheduling techniques to find performance factors.
3. Explain organization of file systems and IOCS.
4. Apply suitable techniques for contiguous and non-contiguous memory allocation.
5. Describe message passing, deadlock detection and prevention methods.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is 50%.The minimum passing mark for the CIE is 40%of the maximum marks(20marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the endof the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to50 marks

Suggested Learning Resources:

TEXT BOOKS

Operating Systems – A concept based approach, by Dhamdhere, TMH, 2nd edition.

REFERENCEBOOKS:

1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.

Web links and Video Lectures(e-Resources):

- **https://archive.nptel.ac.in/courses/106/105/106105214/**
- **https://onlinecourses.nptel.ac.in/noc20_cs04/preview**
- **https://onlinecourses.nptel.ac.in/noc21_cs72/preview**
- **https://nptel.ac.in/courses/106106144**

Data Structures Using C		Semester	IV
Course Code	BEC405D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

COURSE OVERVIEW:

COURSE OBJECTIVES:

The objectives of this course are to:

1. Develop proficiency in designing and implementing fundamental data structures.
2. Learn various sorting and searching algorithms and analyze their time complexity.
3. Understand algorithmic problem-solving techniques, including recursion.
4. Explore advanced data structures like trees, graphs, and hash tables.
5. Apply data structures and algorithms knowledge to solve real-world programming challenges efficiently.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The lecturer's approach (L) does not have to be limited to traditional methods of teaching. It is possible to incorporate alternative and effective teaching methods to achieve the desired outcomes.
2. Utilize videos and animations to illustrate the functioning of different techniques used in the manufacturing of smart materials.
3. Foster collaborative learning exercises within the classroom to encourage group participation and engagement.
4. Pose a minimum of three Higher Order Thinking (HOT) questions during class discussions to stimulate critical thinking among students.
5. Implement Problem-Based Learning (PBL) as an approach that enhances students' analytical skills and nurtures their ability to design, evaluate, generalize, and analyze information, rather than solely relying on rote memorization.

Module-1

Arrays:1D,2D and multidimensional.
Pointers: Definition and Concepts, Array of pointers, Structures and unions. Array of structures, pointer arrays, pointer to structures. Passing pointer variable as parameter in functions
Dynamic memory allocation: malloc(), calloc(), realloc() and free function.
Introduction to data structures and algorithms
Text book 1 -Chapter-1.1-1.3 except Rational Numbers.
Text Book 2, chapter-2

Module-2
The Stack – Definition and examples, primitive operations, Example. Representing Stacks in C, Example:Infix,Postfix and Prefix,converting an Expression from Infix to Prefix and Program. Text Book -1-Chapter – 2.1-2.3 Recursion – Recursive Definition and Processes, Recursion in C, Writing Recursive Programs. Recursions - Text Book -1-Chapter – 3.1-3.3
Module-3
Queues and Lists – The Queue and its sequential representation, Linked Lists, Lists in C. Other Lists structures – Circular Lists, Stacks, Queues as circular list. The Josephus problem ,doubly linked lists. Linked lists and Queues - Text Book -1-Chapter – 4.1-4.3,4.5
Module-4
Trees – Binary Trees, binary tree representations, Huffman algorithm, Trees and their applications. Searching – Basic searching Techniques, Tree Searching. Trees - Text Book -1-Chapter – 5.1-5.3,5.5,7.1,7.2
Module-5
Hashing – Introduction, Static Hashing, Dynamic Hashing Text Book 3 -8.1 – 8.3 Graphs - Graph representation, Elementary graph operations, Minimum cost spanning Trees – Kruskal's Algorithm, Prim's algorithm Text Book 3 - 6.1,6.2,6.3.1,6.3.2
Course Outcomes (COs) (Course Skill Set) At the end of the course, the student will be able to: 1. Master the implementation and application of key data structures in programming. 2. Demonstrate the ability to analyze algorithm efficiency and optimize code. 3. Solve complex problems by applying algorithmic strategies and techniques. 4. Design and implement algorithms for tasks involving searching, sorting, and graph traversal. 5. Utilize data structures and algorithms to enhance software performance and scalability

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shallbe deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the InternalAssessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-basedthen only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination (SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with commonquestion papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (witha maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

TEXT BOOKS:

1. Data Structures using C and C++, Yedidyah, Augenstein, Tannenbaum, 2nd Edition, Pearson Education, 2007.
2. Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
3. Fundamentals of Data structures in C, 2nd Edition, Horowitz, Sahni, Anderson freed Universities Press,2008

REFERENCEBOOKS:

1. Reema Thareja, Computer fundamentals and programming in C, second edition, Oxford University Press.
2. Gilberg and Forouzan, Data Structures: A Pseudo-code approach with C, 2ndEd, CengageLearning,2014.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/102/106102064/
- https://archive.nptel.ac.in/courses/106/106/106106127/
- https://nptel.ac.in/courses/106102064
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS35.html
- https://nptel.ac.in/courses/106/105/106105171/
- http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS43.html
- https://nptel.ac.in/courses/106/101/106101060/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Real world problem solving using group discussion.

- Back/Forward stacks on browsers.
- Undo/Redo stacks in Excel or Word.
- Linked list representation of real-world queues -Music player, image viewer
- Real world problem solving and puzzles using group discussion. E.g., Fake coin identification, Peasant, wolf, goat, cabbage puzzle, Konigsberg bridge puzzle etc.,
- Demonstration of solution to a problem through programming.

Assessment Details(both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor10marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and these test shall be conducted after the 14^{th}week of the semester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40%of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

SEE marks for the practical course is 50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the question slot prepared by the internal/external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20% of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Textbooks:

- Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
- Introduction to the Design and Analysis of Algorithms, Anany Levitin: 2nd Edition, 2009.Pearson.

- Online Courses:
  - Coursera: "Algorithms" by Princeton University (taught by Robert Sedgewick and Kevin Wayne).
  - edX: "Algorithmic Design and Techniques" (offered by UC San Diego and Higher School of Economics).
- Websites and Online Resources:
  - Geeks for Geeks: Offers a wide range of tutorials, practice problems, and coding challenges related to data structures and algorithms.
  - Leet Code: Provides coding challenges that are frequently asked in technical interviews and cover a

variety of algorithmic concepts.
    - Hacker Rank: Offers coding challenges and competitions with a focus on algorithms and data structures.
    - Top Coder: Provides algorithmic challenges and competitions for practicing and improving problem-solving skills.
- YouTube Channels:
    - My code school: Offers video tutorials on various data structures and algorithms topics.
    - The Coding Train: Provides interactive coding tutorials on algorithms and data structures.
- Coding Platforms:
    - Code forces: Offers competitive programming challenges to improve algorithmic problem-solving skills.

  Hackerearth: Provides coding competitions and challenges along with tutorials and practice problems.

Microcontrollers Lab		Semester	4
CourseCode	**BECL456A**	CIEMarks	50
TeachingHours/Week(L:T:P)	0:0:2	SEEMarks	50
Credits	01	TotalMarks	100
		ExamHours	2
Examination type(SEE)	Practical		

Courseo bjectives: This course will enable students to:

- Understand the basic programming of Microcontrollers.
- Developthe8051 Microcontroller-basedprogramsforvariousapplicationsusing Assembly Language & C Programming.
- Program8051Microcontrollertocontrolanexternalhardwareusingsuitable I/Oports.

Note	Execute the following experiments by using Keil Microvision Simulator (any 8051 Microcontroller can be chosen as the target) and Hardware Interfacing Programs using 8051 Trainer Kit.
Sl.No	**I. Assembly Language Programming**
Data Transfer Programs:	
1	Write an ALP to move a block of n bytes of data from source (20h) to destination (40h) using Internal-RAM.
2	Write an ALP to move a block of n bytes of data from source (2000h) to destination (2050h) using External RAM.
3	Write an ALP To exchange the source block starting with address 20h, (Internal RAM) containing N (05) bytes of data with destination block starting with address 40h (Internal RAM).
4	Write an ALP to exchange the source block starting with address 10h (Internal memory), containing n (06) bytes of data with destination block starting at location 00h (External memory).
Arithmetic & Logical Operation Programs:	
5	Write an ALP to add the byte in the RAM at 34h and 35h, store the result in the register R5 (LSB) and R6 (MSB), using Indirect Addressing Mode.
6	Write an ALP to subtract the bytes in Internal RAM 34h &35h store the result in register R5 (LSB) & R6 (MSB).
7	Write an ALP to multiply two 8-bit numbers stored at 30h and 31h and store16- bit result in 32h and 33h of Internal RAM.
8	Write an ALP to perform division operation on 8-bit number by 8-bit number.
9	Write an ALP to separate positive and negative in a given array.
10	Write an ALP to separate even or odd elements in a given array.
11	Write an ALP to arrange the numbers in Ascending & Descending order.
12	Write an ALP to find Largest & Smallest number from a given array starting from 20h & store it in Internal Memory location 40h.
Counter Operation Programs:	
13	Write an ALP for Decimal UP-Counter.
14	Write an ALP for Decimal DOWN-Counter.
15	Write an ALP for Hexadecimal UP-Counter.
16	Write an ALP for Hexadecimal DOWN-Counter.
	II. C Programming
1	Write an 8051 C program to find the sum of first 10 Integer Numbers.
2	Write an 8051 C program to find Factorial of a given number.
3	Write an 8051 C program to find the Square of a number (1 to 10) using Look-Up Table.
4	Write an 8051 C program to count the number of Ones and Zeros in two consecutive memory locations.
	III. Hardware Interfacing Programs
1	Write an 8051 C Program to rotate stepper motor in Clock & Anti-Clockwise direction.
2	Write an 8051 C program to Generate Sine & Square waveforms using DAC interface.

Courseoutcomes(CourseSkillSet): Attheendofthecoursethestudentwillbeableto:

1. Write a Assembly Language/Cprogramsin8051forsolvingsimpleproblemsthatmanipulateinputdatausingdifferentinstructions.
2. Develop Testing and experimental procedures on 8051 Microcontroller, Analyze their operation under different cases.
3. Developprogramsfor8051Microcontrollertoimplementreal worldproblems.
4. DevelopMicrocontrollerapplicationsusingexternalhardwareinterface.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimumpassing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied theacademic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester EndExamination)takentogether.

ContinuousInternalEvaluation(CIE):

CIEmarksforthepracticalcourseare**50Marks**.

ThesplitupofCIEmarksforrecord/journalandtestareintheratio**60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics fortheevaluationofthejournal/write-upforhardware/softwareexperimentsaredesignedbythefacultywhoishandlingthelaboratorysessionandaremadeknowntostudentsatthebeginningofthepracticalsession.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor 10marks.
- Totalmarksscoredbythestudentsarescaleddownto **30marks**(60%ofmaximummarks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upontime.
- Departmentshallconductatestof100marksafterthecompletionofalltheexperimentslistedinthesyllabus.
- Inatest,testwrite-up,conductionofexperiment,acceptableresult,andproceduralknowledgewillcarryaweightageof 60%andthe rest40%forviva-voce.
- Thesuitablerubricscanbedesignedtoevaluateeachstudent'sperformanceandlearningability.
- Themarksscoredshallbescaleddownto**20marks**(40%ofthemaximummarks).

TheSumofscaled-downmarksscoredinthereportwrite-up/journalandmarksofatestisthetotalCIEmarksscored bythe student.

SemesterEndEvaluation(SEE):

- SEEmarksforthepractical courseare50Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointedbytheHeadof theInstitute**.
- The examination schedule and names of examiners are informed to the university before the conduction ofthe examination. These practical examinations are to be conducted between the schedule mentioned in theacademiccalendar of the University.
- Alllaboratoryexperimentsaretobeincludedforpracticalexamination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to bestrictly adhered to by the examiners.**OR** based on the course requirement evaluation rubrics shall bedecidedjointlybyexaminers.
- Studentscanpickonequestion(experiment)fromthequestionslotpreparedbytheexaminersjointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,Viva-voce20%ofmaximummarks.SEEforpracticalshallbeevaluatedfor100marksandscoredmarksshallbescaleddownto 50marks(however,basedoncoursetype,rubricsshallbedecidedby the examiners)

Changeofexperimentisallowedonlyonceand15%ofMarksallottedtotheprocedurepartaretobemadezero.Theminimum durationofSEEis02hours

SuggestedLearningResources:

"The 8051 Microcontroller: Hardware, Software and Applications" ,V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education,1st edition,2017.

PROGRAMMABLE LOGIC CONTROLLER (PLC)		Semester	IV
Course Code	**BEC456B**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	14 to 16 hours	Total Marks	100
Credits	01	Exam Hours	01
Examination type (SEE)	Theory		

Course objectives: This course will enable student to

- To understand the need for automation in the industry with basic controller mechanisms involved.
- To study programming concepts to achieve the desired goal or to define the various steps involved in the automation.
- To understand programming involved with basic subroutine functions.
- To make use of the internal hardware circuits of automation circuit to control the devices during various states by monitoring the timers and counters.
- To handle the data of the I/O devices to interface the data with the controller and auxiliary devices.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Programmable logic controller (PLC), role in automation (SCADA), advantages and disadvantages, hardware, internal architecture, sourcing and sinking **(Textbook 1: 1.1 to 1.4)**

I/O devices and Processing: list of input and output devices, examples of applications. I/O processing, input/output units, signal conditioning, remote connections, networks, processing inputs I/O addresses. **(TextBook1: 2.1 to 2.3 and 4.1 to 4.7).**

Module-2

Programming: Ladder programming- ladder diagrams, logic functions, latching, multiple outputs, entering programs, functional blocks, program examples like location of stop and emergency switches. (**TextBook1: 5.1 to 5.7).**

Module-3

Programming Methods: Instruction Lists- Ladder programs and Instruction lists, Branch codes, Programming Examples- Signal lamp-valve operation task. Sequential Function Charts- Branching and convergence. **(TextBook1: 6.1 to 6.3).**

Module-4

Internal Relays: ladder programs, battery-backed relays, one-shot operation, set and reset, master control relay (**TextBook1: 7.1 to 7.6).**

Timers and counters: Types of timers, ON and OFF- delay timers, pulse timers, forms of counter, programming, up and down counters. **(TexBook1: 9.1 to 9.6).**

Module-5

Shift register and data handling: shift registers, ladder programs, registers and bits, data handling, arithmetic functions. **(TextBook1: 11.1 to 11.2 and 12.1 to 12.3)**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the PLC and how to construct PLC ladder diagrams.
2. Illustrate an application with programming.
3. Describe characteristics of registers and conversion examples.
4. Apply PLC functions to timing and counting applications.
5. Analyse the analog operation of PLC and demonstrate the robot applications with PLC.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned.
- The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 01 hours).**

1. SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions).
2. The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Textbooks:

1. Programmable Logic controllers-W Bolton, 5th edition/6th edition, Elsevier- newness, 2009/2015.
2. Programmable logic controllers - principles and applications"-John W. Webb, Ronald A Reiss, Pearson education, 5th edition, 2007.

Reference Books:

1 Programmable Logic Controllers"- E. A Paar, 3rd Edition, An Engineers Guide. Newness, 2003.
2 "Introduction to Programmable Logic Controller"- Garry Dunning, 3rd Edition, Thomson Asia Pte Ltd. Publication, 2006
3 "PLCs & SCADA - Theory and Practice"- Rajesh Mehra, Vikrant Vij, 2nd Edition, Laxmi publication, 2017
4 "PLC Programming for Industrial Automation"- Kevin Collins, 1st Edition, Kindle, 2016

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning.

- Quiz and Seminars

Octave Programming			
Course Code	**BECL456C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2	SEE Marks	50
Total Hours of Pedagogy	12 Sessions	Total	100
Credits	01	Exam Hours	02

**Additional One hour may be considered for instructions if required*

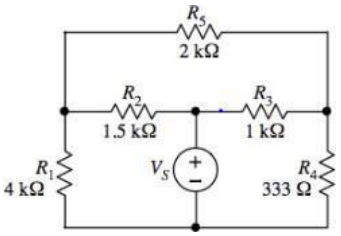
Course objectives:

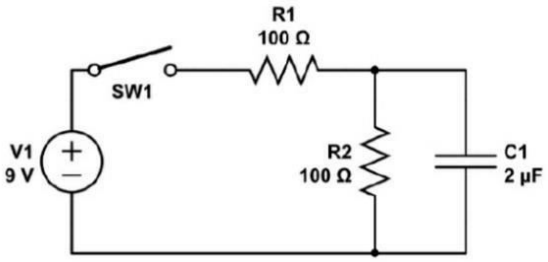
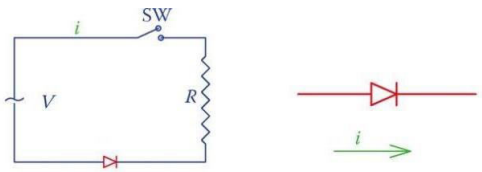
- Apply theoretical knowledge of Octave programming to practical programming tasks.
- Gain hands-on experience in implementing and debugging octave Programming through coding exercises and projects.

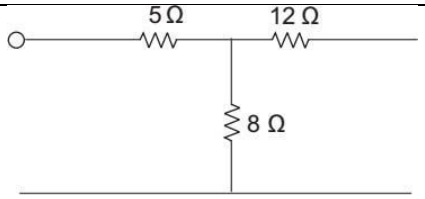
Course Syllabus :

Basic data structures in Octave – Vectors, Matrices, Cell Arrays. Special vecors. Linear sampling and logarithmic sampling. Accessing elements of vectors, matrices, and matrices. Mathematical operations on vectors and matrices. Addition, Multiplication, Subtraction, Division, Power, Square-Root, trigonometric operations. Dot Products and Cross Products of Vectors. Matrix multiplication, matrix inverse and matrix transpose operations. Finding eigen values and vectors of a square matrix. Finding the solution of a system of linear equations. Linear programming and integer linear programming using glpk. Plotting in Octave. Subplots, Stem Plots, Semilog and Log-log plots. Packages in Matlab – symbolic, signal processing, control. Applications of Octave to solve problems in Electrical engineering, Electronics engineering, Control Systems, Signals and Systems/Signal Processing.

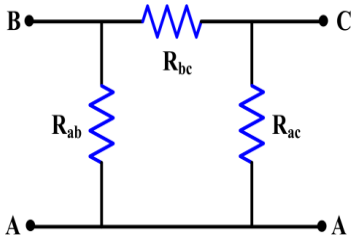
Sl..NO	Experiments
1	(a) Define the following matrices using Octave i. A 4x4 identity matrix ii. A 4x4 matrix of zeros iii. A 4x4 matrix of ones iv. The matrix U4 defined below. 1 2 3 4 2 3 1 4 1 3 2 4 4 3 1 2 v. Matrix D4 defined below. It is also called the Hadamard matrix of dimension 4. 1 1 1 1 1 -1 1 -1 1 1 -1 -1 1 -1 -1 1 vi. Matrix H4 defined below $\mathbf{H}_4 = \frac{1}{\sqrt{4}}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ \sqrt{2} & -\sqrt{2} & 0 & 0 \\ 0 & 0 & \sqrt{2} & -\sqrt{2} \end{bmatrix}$ vii. A 4x4 magic square G4 viii. A 4x4 matrix of random numbers selected from the range {-1,0,1}. ix. A 4x4 matrix of random numbers in the range 0 to 1. (b) (i) How can you generate a 4x4 matrix of all 2's? (ii) Find the transpose of U4. (iii) Multiply D4 by its transpose and obtain the resulting matrix. How is

	related tothe identify matrix? (iv) Find the inverse of H4 and verify that it is the inverse. (v) What is the determinant of D4? (vi) Extract the diagonal elements of H4. (vii) How can you reshape the elements of D4 into a 2x8 matrix? (viii) What is the magic sum of a 4x4 matrix? How can you verify that G4 is indeed amagic square? (ix) The matrix D4 mentioned above is a 4x4 matrix. We wish to extract the sub-matrix consisting of rows 1 and 4 and columns 1 and 4. [In other words, the four corners of D4.) Show Octave code for generating the submatrix SM. (x) Check if the H4 and D4 are orthogonal matrices.
2	You will have learnt Kirchhoff's current and voltage laws to solve the voltages and currents in a DC circuit. Given a circuit with n loops, we can write down n equations in n unknowns (loop currents). Alternately, given a circuit with n nodes, we can write down n equations in n unknowns (node voltages). These linearequations can be solved using Octave. (a) Write down the KCL and KVL for the following circuit and solve the node voltages and currents. Assume that Vs is 100V.  (b) Find the total power dissipated in the circuit. (c) Find the total power supplied by the voltage source. (d) Challenge – Instead of hardcoding the values of the resistors and the voltage source, can you allowthe user to input R1, R2, R3, R4, R5, and Vs? Develop a complete Octave script which reads in the values of circuit parameters and prints the node voltages, node currents, and power dissipation. (e) Variations of the above exercises can be given to the students. For example, a resistor can be included in series with Vs. Alternately, a different circuit from a text book can be given. You can alsochange the problem by specifying the current through one of the resistors and asking the user to solve for Vs.
3	(a) Consider the RC circuit shown in the figure below. Plot the voltage across C and the chargingcurrent through C when the switch is turned on. (b) What is the rise time of the capacitor voltage?

	
4	 (a) The figure shows a diode-based rectifier. The diode conducts only when the input voltage is positive. Assume that it is an ideal diode. Plot the half-wave rectified waveform if the input to the rectifier is a 50-Hz sine wave of 200V RMS. Plot the output waveform for four cycles of the input. (b) Find the average of the Halfwave-rectified output in Octave and verify your answer using the formula forthe average output. (c) Plot the output of a full-wave rectifier. (d) Find the RMS value of the Fullwave-rectified output in Octave and verify your answer using the formulafor the RMS value. (e) Assume that the input voltage is 2sin(500t) V and that the diode has a cut-in voltage of 0.6V. Plot thehalf-wave and full-wave rectified waveforms and find their average and RMS values.
5	You have studied that any periodic signal of frequency f can be decomposed into a sum of sine and cosinewaveforms whose frequencies ae integral multiples of f. The resulting series is called the Fourier series. Consider the following equation. $$\boldsymbol{x(t) = 4/\pi \times \sum\_(k = 1)\text{^}n\ [\![sin\ (2\ \pi f\ (2k - 1)t)\ ]\!]}$$ (a) Write an Octave program to read f and n and plot x(t). What does x(t) resemble? (b) How can you modify x(t) to generate a square waveform of frequency f, but whose amplitude goes from 0 to 2? (c) Generate x(t) assuming that the square wave goes from -1 to 1 and has a frequency of 1 kHz. Take 100 samples in each period. Perform an FFT analysis of x(t).
6	(a) Given Z parameters, obtain the Y parameters using a function called Z2Y()Given Y parameters, obtain the Z parameters using a function called Y2Z() (b) Find the Z and Y parameters for the T-network



(c) Find the Z and Y parameters for the Delta. Assume that all resistors are 15 Ohms.



(d) Find the T-equivalent of the Delta network above.

(e) Find the T-equivalent of the Delta network above. Let the T network have the resistors Zb, Zc, Za.

7

(a) Represent the number 65 as an unsigned integer using fewest number of bits
(b) Represent the number -65 as a signed magnitude integer using the fewest number of bits
(c) Represent the number -65 as a one's complement number using fewest number of bits
(d) Represent the number -65 as a two's complement number using the fewest number of bits
(e) Represent the number 1965 in hexadecimal
(f) Find the decimal equivalent of the hexadecimal number ABCDh
(g) Assume that "10010101" is a binary number. Interpret it as an unsigned number and convert it todecimal.
(h) Memory is organized in terms of bytes. When a 32-bit number is read from a memory, 4 bytes haveto be read. Suppose the bytes are stored as follows at location A in the memory. In the little-endian representation, the bytes will be organized into a 32-bit register as shown. Write a function which converts a 32-bit number from big-endian to little-endian format.

MEM LOC M	00h
MEM LOC M+1	01h
MEM LOC M+2	02h
MEM LOC M+3	03h
MEM LOC M+4	04h
…	…

03	02	01	00

Little Endian

02 03

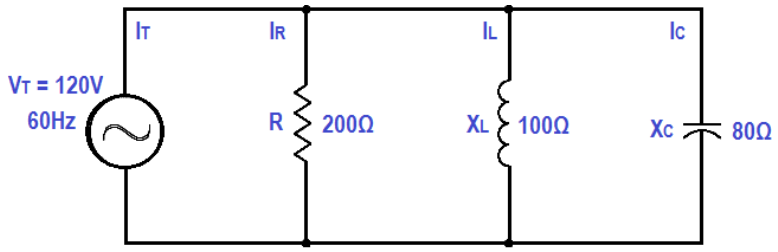
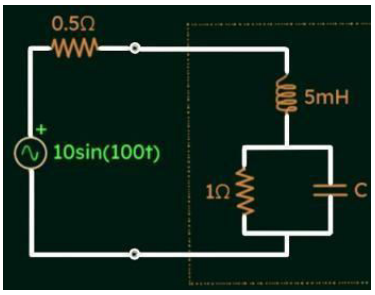
00 01

Big Endian

8

A series circuit consists of resistance R, inductance L and capacitance C. A sinusoidal voltage of V sin(wt) isapplied to the series circuit. Assume V=100. Plot the current in the circuit and the input voltage for the following cases.

(a) w=1000, R = 5 ohm, L = 1mH, C = 200uF; is the current leading or lagging? What is the powerdissipation in the circuit?
(b) w=10000, R=5 ohm, L = 1mH, C = 200 uF; is the current leading or lagging? What is the powerdissipation in the circuit?
(c) The resonant frequency w0, R = 5 ohm, L = 1mH, C = 200uF. What is the phase difference betweenthe voltage and current? What is the value of w? What is the power dissipation?

	Write a function to plot the voltage and current. Take the inputs R, L, and C from the user.
9	(a) Consider the circuit shown below and determine the inductance L and capacitance C. (b) Plot the impedance of the RLC circuit shown in the figure as the frequency is varied from 0 to 10kHz. (c) Find the resonant frequency from the plot  (a) Parallel RLC Circuit
10	Find the value of capacitor C to maximize the power transferred to the load. (The load includes  theinductance.) **Course outcomes (Course Skill Set):** At the end of the course the student will be able to: ● Develop proficiency in octave coding and debugging complex program flow. ● Understand the concepts of Matrices and apply the octave programming concepts to solve the Matrices. ● Acquire practical knowledge and apply the octave programming skills to solve Electric circuits. ● Develop a Octave program to analyze the continuous and discrete signals ● Understand the concept memory and to represent data and address using Octave Programming.
	Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). **Continuous Internal Evaluation(CIE):** CIE marks for the practical course is **50 Marks**. The split-up of CIE marks for record/journal and test are in the ratio **60:40**. • Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratory session and is made known to students at the beginning of the practical session. • Record should contain all the specified experiments in the syllabus and each experiment

	write-up willbeevaluatedfor10marks. • Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks). • Weightage to be given for neatness and submission of record/write-upon time. • Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of thesemester and these test shall be conducted after the 14thweek of the semester. • In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry aweightage of 60% and the rest 40% for viva-voce. • The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubricssuggested in Annexure-II of Regulation book • The average of 02 tests is scaled down to **20 marks** (40%of the maximum marks). The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marksscored by the student.
	Semester End Evaluation(SEE): SEE marks for the practical course is 50Marks. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the UniversityAll laboratory experiments are to be included for practical examination. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adheredto by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners. Students can pick one question (experiment) from the question slot prepared by the internal/external examiners jointly.Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. Theduration of SEE is 03hours Rubrics suggested in Annexure-II of Regulation book
	Suggested Learning Resources: Textbooks: Dr. P.J.G. Long, Department of Engineering University of Cambridge, "Introduction to Octave," can be downloaded from octavetut.pdf (cam.ac.uk)

Data Structures Lab using C			
Course Code	BECL456 D	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2	SEE Marks	50
Total Hours of Pedagogy	15 Sessions	Total	100
Credits	01	Exam Hours	03

Additional One hour may be considered for instructions if required

Course objectives:

- Apply theoretical knowledge of data structures and algorithms to practical programming tasks.
- Gain hands-on experience in implementing and debugging data structures and algorithms through coding exercisesand projects.

Sl..NO	Experiments
1	Write a C Program to create a Student record structure to store, N records, each record having the structure shown below: USN, Student Name and Semester. Write necessary functions a. To display all the records in the file. b. To search for a specific record based on the USN. In case the record is not found, suitable message should be displayed. Both the options in this case must be demonstrated. (Use pointer to structure for dynamic memory allocation)
2	Write a C Program to construct a stack of integers and to perform the following operations on it: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow, stack underflow, and stack empty.
3	Write a C Program to convert and print a given valid parenthesized infix arithmetic expression to postfix expression. The expression consists of single character operands and the binary operators + (plus), - (minus), * (multiply) and / (divide).
4	Write a C Program to simulate the working of a queue of integers using an array. Provide the following operations: a. Insert b. Delete c. Display
5	Write a C Program using dynamic variables and pointers to construct a stack of integers using singly linked list and to perform the following operations: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow and stack empty.
6	Write a C Program to support the following operations on a doubly linked list where each node consists of integers: a. Create a doubly linked list by adding each node at the front. b. Insert a new node to the left of the node whose key value is read as an input c. Delete the node of a given data, if it is found, otherwise display appropriate message. d. Display the contents of the list. (Note: Only either (a,b and d) or (a, c and d) may be asked in the examination)
7	Write a C Program a. To construct a binary search tree of integers. b. To traverse the tree using all the methods i.e., inorder, preorder and postorder. c. To display the elements in the tree.
8	Write recursive C Programs for a. Searching an element on a given list of integers using the Binary Search method. b. Solving the Towers of Hanoi problem.
9	Write a program to traverse a graph using BFS method. Write a program to check whether given graph is connected or not using DFS method.
10	Design and develop a program in C that uses Hash Function H:K->L as H(K)=K mod m(reminder method) and implement hashing technique to map a given key K to the address space L. Resolve the collision (if any) using linear probing

Note: The students must be encouraged to create Leetcode account and work on Leetcode platform to improve the competency.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Develop proficiency in coding and debugging complex algorithms and data structures.
- Acquire practical problem-solving skills by applying data structures and algorithms to real-world programming challenges.
- Develop a C program to perform arithmetic operation using data structure and operators.
- Understand the concept of graph theory and develop a C program for searching an element.
- Develop a C program to check the given graph is connected using different algorithms.

Assessment Details(both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor10marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and these test shall be conducted after the 14^{th}week of the semester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40%of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

SEE marks for the practical course is 50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the question slot prepared by the internal/external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20% of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Textbooks:

- Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
- Introduction to the Design and Analysis of Algorithms, Anany Levitin: 2nd Edition, 2009.Pearson.

- Online Courses:
  - Coursera: "Algorithms" by Princeton University (taught by Robert Sedgewick and Kevin Wayne).
  - edX: "Algorithmic Design and Techniques" (offered by UC San Diego and Higher School of Economics).
- Websites and Online Resources:
  - Geeks for Geeks: Offers a wide range of tutorials, practice problems, and coding challenges related to data structures and algorithms.
  - Leet Code: Provides coding challenges that are frequently asked in technical interviews and cover a

variety of algorithmic concepts.
    - Hacker Rank: Offers coding challenges and competitions with a focus on algorithms and data structures.
    - Top Coder: Provides algorithmic challenges and competitions for practicing and improving problem-solving skills.
- YouTube Channels:
    - My code school: Offers video tutorials on various data structures and algorithms topics.
    - The Coding Train: Provides interactive coding tutorials on algorithms and data structures.
- Coding Platforms:
    - Code forces: Offers competitive programming challenges to improve algorithmic problem-solving skills.

  Hackerearth: Provides coding competitions and challenges along with tutorials and practice problems.

	Embedded System Design	Semester	06
Course Code	BEC601	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory		

Course objectives:

- Identify various components, their purpose, and their application to the embedded system's applicability.
- Program various embedded components using the embedded C program.
- Understand the embedded system's real-time operating system and its application in IoT
- Understand the fundamentals of ARM-based systems, including architecture and its units like registers , debug interface, stack, MPU, Interrupts etc
- Use the various instructions to program the ARM controller.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

MODULE-1

Introduction to Embedded System: What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Major Application Areas of Embedded Systems. Purpose of Embedded Systems, The Typical Embedded System, Microprocessor Vs Microcontroller, Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors, Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7-Segment LED Display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface, External Communication Interface, Embedded Firmware, Other System Components

(Text 1: All the Topics from Ch-1 and Ch-2.)

MODULE-2

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).

Text 1: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)
MODULE-3
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil). **(Text 1: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2 only), Ch-12, Ch-13 (a block diagram before 13.1, only).**
MODULE-4
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2: Chapter 1, 2**
MODULE-5
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2: Chapter 3**

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn Assembly Language Program and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

Sl.NO	Experiments
1	Write a program to find the sum of the first 10 integer numbers.
2	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3	Write a program to find the factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5	Write a program to find the square of a number (1 to 10) using a look-up table.
6	Write a program to find the largest or smallest number in an array of 32 numbers.
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	Write a program to count the number of ones and zeros in two consecutive memory locations.
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Understand the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. **Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education**
2. **Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.**

Reference Book

1. **Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.**

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105193/
2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference
3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/
4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors
5. https://alison.com/tag/embedded-systems

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

`

	VLSI Design and Testing	Semester	5
Course Code	**BEC602**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1.This course deals with analysis and design of digital CMOS integrated circuits.

2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.

3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.

4. Understanding the CMOS sequential circuits and memory design concepts.

5.Explore the knowledge of VLSI Design flow and Testing

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.

[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

`

Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3.

MODULE-3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.
[Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:
Chalk and talk method/Power point presentation, YouTube Videos RBT Level: L1, L2, L3.

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.

[Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:
Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.
[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction**,** Design Styles, Testing
[Text1: 6.1, 6.2. 6.5]

Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Course Outcomes: After completing the course, the students will be able to

`

CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
C05	Understand the concepts of Sequential circuits design and VLSI testing

`

	Multimedia Communication		Semester	6
	Course Code	**BCE613A**	CIE Marks	50
	Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	
	Examination type (SEE)	Theory		

Course objectives:

- Gain fundamental knowledge in understanding the basics of different multimedia Networks and applications.
- Understand digitization principle techniques required to analyze different media Types.
- Analyze compression techniques required to compress text and image and gain Knowledge of DMS.
- Analyze compression techniques required to compress audio and video.
- Gain fundamental knowledge about multimedia communication across different Networks.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text1)

Module-2

Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1

Module-3

Text and Image Compression: Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1)

Module-4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)

Module-5

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI (Chapter 8.1 to8.6of Text 1).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the basics of multimedia Communication and applications
2. Analyze media types to represent them in digital form.
3. Apply the compression techniques on text, images, audio and video.
4. Understand multimedia information networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks:

Multimedia Communications –Fred Halsall, Pearson Education,2001,ISBN-978813170994

ReferenceBooks:

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. FundamentalsofMultimedia–Ze-NianLi,MarkSDrew,andJiangchuanLiu.

Web links and Video Lectures (e-Resources):

- Implementation of compression algorithms using MATLAB/any open source tools (Python, Scilab, etc.)

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- https://www.slideshare.net
  NPTEL Video Lectures
- https://archive.nptel.ac.in/courses/117/105/117105083/
- Multimedia Computing lecture: Communications & Networking –You Tube

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

Data Security

Course Code	**BEC613B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
CREDITS - 03			

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, authentication functions like HASH codes, MACs, digital signatures, as well as key distribution

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1	RBTL Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques (excluding Hill cipher) (Text 1: Chapter 1: Section 1, 2) **Block Ciphers**: Traditional Block Cipher structure, (Text 1: Chapter 2: Section1) The AES Cipher. (Text 1: Chapter 4: Section 2,4) Block Cipher Modes of Operation (Text 1: Chapter 5: Section 2, 3, 4, 5, 6)	L1, L2, L3
MODULE-2	
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Fields of the Form GF(2_m) (Text 1: Chapter 3)	L1, L2, L3
MODULE-3	

More on Number Theory: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5) **ASYMMETRIC CIPHERS**: Principles of Public-Key Cryptosystems, The RSA algorithm (Text 1: Chapter 8: Section 1, 2), Diffie – Hellman Key Exchange, Elliptic Curve Arithmetic over Z_p, Elliptic Curve Cryptography (Text 1: Chapter 9: Section 1, 3, 4)	L1, L2, L3
MODULE-4	
Cryptographic Hash Functions: Application of Hash Functions, Two Simple Hash Functions, Requirements and Security, Hash function based on Cipher Block Chaining, SHA-512 (Only structural description). (Text 1: Chapter 10: Section 1, 2, 3, 4, 5) **Message Authentication Codes:** Message Authentication Functions, Security of MACs, MACs based on Hash Functions. (Text 1: Chapter 11: Section 2, 4, 5)	L1, L2, L3
MODULE-5	
Digital Signatures: Digital Signatures, NIST Digital Signature Algorithm, Elliptic Curve Digital Signature Algorithm. (Text 1: Chapter 12: Section 1, 4, 5) **Key Management and Distribution:** Symmetric Key Distribution Using Symmetric Encryption, Symmetric Key Distribution Using Asymmetric Encryption, Distribution of Public Keys (Text 1: Chapter 13: Section 1, 2, 3)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain traditional cryptographic algorithms of encryption and decryption process.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
- Apply concepts of modern algebra in cryptography algorithms.
- Explain message authentication using HASH functions, MAC functions and Digital signatures.
- Explain how symmetric and asymmetric encryption algorithms can be used to distribute keys.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

Reference Books

1. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
2. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/105/106105162

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VI Semester

Digital Image Processing			
Course Code	**BEC613C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

<table>
<tr><th colspan="2">Module-2</th></tr>
<tr><td colspan="2">Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform.
Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications.
Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform.
Practical topics: Problems on DFT and DCT
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-3</th></tr>
<tr><td colspan="2">Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
[Text: Chapter 3: Sections 3.2 to 3.6]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters.
Self-study topics: Point, line and edge detection.
Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-4</th></tr>
<tr><td colspan="2">Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.
Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.
[Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing.
Self-study topics: Basic concept of segmentation.
Practical topics: Problems on Pseudo-color Image Processing
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-5</th></tr>
<tr><td colspan="2">Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and their applications.
Self-study topics: Linear position invariant degradation, Estimation of degradation function.
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="2">Course outcomes (Course Skill Set)
At the end of the course the student will be able to:
1. Understand image formation and the role of human visual system plays in the perception of gray andcolor image data.
2. Compute various transforms on digital images.
3. Conduct an independent study and analysis of Image Enhancement techniques.
4. Apply image processing techniques in the frequency (Fourier) domain.
5. Design image restoration techniques.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based Learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

FPGA Based System design Using Verilog		Semester	VI
Course Code	BEC613D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various courseoutcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different types of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction to Programmable Logic Devices:

Hazards in Combinational Circuits, Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs)
Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)

(Text 1: 1.5,3.1,3.2 , 3.3, 3.4) RBT Level: L1, L2, L3

Module-2

Advanced Digital Design Examples:
BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light controller, Synchronization and debouncing, Shift-and-Add Multiplier
Array Multiplier, A Signed Integer/Fraction Multiplier, (Excluding Test Bench) , Keypad Scanner (Excluding Test Bench)

Module-3

SM Charts and Microprogramming :
State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier , Dice Game (Excluding Test Bench) , Realization of SM Charts , Implementation of the Dice Game . Microprogramming , Linked State Machines.
(**Text 1: 5.1, 5.2, 5.3 , 5.4 , 5.5 , 5.6) RBT Level:** L1, L2, L3

Module-4

Floating-Point Arithmetic: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations.
Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Rise and Fall Delays of Gates

(Text 1:7.1,7.2, 7.3,7.4, 8.3, 8.4, 8.5,8.6,8.8) RBT Level: L1, L2, L3

Module-5

Designing with Field Programmable Gate Arrays :
Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition Carry Chains in FPGAs , Cascade Chains in FPGAs , Examples of Logic Blocks in Commercial FPGAs , Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates , Design Translation.

(Text 1: 6.1,6.2,6.3, 6.4 ,6.5 , 6.6, 6.7, 6.8,6.10, 6.11) RBT Level: L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Apply the concept of Programmable logic devices to implement digital design.
2. Design and implementation of Advanced logic design using Verilog HDL
3. Understand the concept of SM Chart and design complex digital circuits using SM Chart.
4. Performing the Floating-point arithmetic operations and designing of Memories
5. Designing and performance evaluation of advanced digital design using FPGAs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1 Digital Systems Design Using Verilog First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John The University of Texas at Austin, Byeong Kil Lee The University of Texas at San Antonio

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum

2. ASIC and FPGA Verification: A guide to component Modelling.
Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier

3. Processor Design . System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland Tampere University of Technology Sringer Publications.

4. The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

Activity Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's

Digital System Design using Verilog		Semester	6
Course Code	**BEC654A**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Functions.
- Understand Timing and Delay Simulation.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

Overview of Digital Design with Verilog HDL: Evolution of Computer-Aided Digital Design (CAD), Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. (**Text 1: 1.1 to 1.6**)

Hierarchical Modeling Concepts: Design Methodologies, Top-down and Bottom-up design methodology, Modules, Instances, Components of a Simulation, Design Block, Stimulus Block (Test Bench) with example. **(Text 1:2.1 to 2.6)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Basic Concepts: Lexical Conventions, Data Types, System Tasks, Compiler Directives. **(Text 1: 3.1 to 3.3)**

Modules and Ports: Modules, Ports, Connecting Ports, Hierarchical Names. **(Text 1: 4.1 to 4.3)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Gate-Level Modeling: Gate Types-Modeling using basic Verilog gate primitives, Description of AND/OR and BUF/NOT type gates. Gate Delays-Rise, Fall and Turn-Off Delays, Min, Max and Typical Delays. **(Text1: 5.1, 5.2)** **Dataflow Modeling**: Continuous assignments, Delay Specification, Expressions, Operators, Operands, Operator Types, Examples **(Text 1: 6.1 to 6.5)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Behavioral Description: Structured Procedures, Initial and Always statements, Procedural Assignments Blocking and Non-Blocking statements, Conditional statements, Multiway Branching, Loops, Sequential and Parallel blocks, Examples-4-to-1 Multiplexer, 4-bit Counter. **(Text 1: 7.1, 7.2, 7.4, 7.5, 7.6, 7.7, 7.9.1, 7.9.2)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Structural Description: Highlights of Structural Descriptions, Organization of Structural Description, Binding **(Text 2: 4.1, 4.2, 4.3, Listings 4.1 to 4.13 only Verilog)** **Tasks and Functions**: Differences between Tasks and Functions, Declaration and Invocation, Examples **(Text 1: 8.1, 8.2, 8.2.1, 8.2.2, 8.3, 8.3.1, 8.3.2)**	

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the Verilog HDL design flow.
2. Describe the basic concepts of Verilog HDL programming.
3. Write Verilog programs in Gate, Dataflow, Behavioral, and structural modeling levels of Abstraction.
4. Write the programs more effectively using Verilog Tasks and Functions.
5. Perform Timing and Delay Simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier

	Consumer Electronics		Semester	6
	Course Code	**BEC654B**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- To understand the working principles and classifications of various microphones and loudspeakers, and their roles in audio systems.
- To explore the structure, recording, and playback processes of Audio Compact Disc systems, along with error correction techniques and digital-to-analog conversion.
- To analyse the fundamentals of colour television systems, including the transmission of colour signals, and to study recent advances in television technology.
- To gain knowledge of modern consumer electronic devices such as mobile phones, home appliances, and computers, focusing on their applications and technological advancements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Microphones: Introduction, Requirements, Quality of Microphones, Classification, Moving Coil Microphone, Ribbon Microphone, Condenser (or Capacitor) Microphone, Crystal Microphone, Carbon Microphone, Electret Microphone.

Loudspeakers: Introduction, Features of Loudspeaker, Moving Coil (Cone Type) Loudspeaker, Electrodynamic Loudspeaker, Horn Loudspeaker, Loudspeaker for High Fidelity Systems.

(Text : 5.1 to 5.10 and 6.1 to 6.6)

Module-2

Audio Compact Disc Systems: Introduction, Comparison of CD and Tape, Optical Recording, Details of a Compact Disc, Details of Recording Process, Details of playback Process, Geometry of Audio Disc, Encoding Process and Error Correction, D/A Convertor, Handling of Compact Disc.

(Text : 10.1 to 10.10)

Module-3

Colour Television: Introduction, Light Energy, Primary Colours, Tristimulus Values, Trichromatic Coefficients, Colour Triangle, Mixing of Colours, Grassman's Law, Colour Specifications, Bandwidth for Colour Signal Transmission. Chromaticity Diagram, Spectral and Non-Spectral Colours, Colour Circle, Visibility Curve, Digital Television (DTV) and High Definition Television (HDTV), Recent Advances in TV technology, LCD TV, LED TV, Plasma TV

(Text : 14.1 to 14.9, 14.13 to 14.16 and 14.26 to 14.27)

Module-4

	Cable Television: Introduction, Video Monitor, Closed Circuit Television (CCTV), Cable Television, Cable TV Using Internet. **Miscellaneous Devices:** Digital Watch, Calculator, An Electronic Guessing Game, Cordless Telephone. (Text : 15.1 to 15.5 and 17.1 to 17.4)
	Module-5
	Mobile Telephone, Cellular Telephone, UPS, Inverter, Decorative Lighting, Remote Control for TV and VCR, Facsimile (FAX), Pager, Microwave Oven, LCD Timer with Alarm, Electronic Ignition System for Automobiles, Washing Machine, Organisation of Digital computer, Microprocessor, Note Book, Laptop, Tablet PC, Ultrabook, IPAD, Recent Advances in Consumer Electronics. (Text : 17.6 to 17.7 and 17.13 to 17.27)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the functioning and classification of various types of microphones and loudspeakers
2. Demonstrate knowledge of the optical recording and playback processes in audio compact disc systems
3. Analyse the principles of colour television and modern display technologies
4. Evaluate the working of cable television systems and miscellaneous consumer devices
5. Explore advancements in consumer electronics, such as mobile phones, computing devices, and home appliances

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. B.R. Gupta, V. Singhal "Consumer Electronics", S.K. Kataria & Sons, 6th edition, 2013, ISBN 978-93-5014-407-7.
2. R.P.Bali, Consumer Electronics, Pearson Education (2008)

Web links and Video Lectures (e-Resources):

- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview
- Microelectronics: Devices to Circuits: https://onlinecourses.nptel.ac.in/noc24_ee139/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Trouble shoot the common consumer electronics products like T.V., Washing machine , microwave oven , FAX, Copier machine.
- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Make visit to service centres of gadgets covered in curriculum and if possible work there for some days on voluntarily basis during holidays.
- Search internet websites for DYS (Do Your Self) repair of electronic gadgets and try your hands to repair some gadgets based on that.

Electronic Communication Systems		Semester	6
Course Code	BEC654C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Describe essential elements of an electronic communication system.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Define the sampling theorem and methods to generate pulse modulations.
- Learn the various methods of digital modulation techniques and compare the different schemes.
- Introduce the basic concepts of information theory and coding.
- Understand the basic concepts of wireless and cellular communications.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)

Module-2

Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6)

Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)

Module-3

Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)

Module-4

Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5)

Information Theory, Source and Channel Coding: Information, Entropy and its properties, Shannon,- Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]

Module-5

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the scheme and concepts of radiation and propagation of communication signals through air.
2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.
3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.
4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.
5. Compare the different wireless communication systems and describe the structure of cellular communication.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1.
2. 2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Reference Books

1. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1
3. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81- 265-4231-4

Web links and Video Lectures (e-Resources):
1. Communication Engineering **https://nptel.ac.in/courses/117102059**
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning 1. Assignments and test – Knowledge level, Understand Level and Apply level 2. Experiential Learning by using free and open source software's SCILAB or OCTAVE or Python

VISVESVARAYATECHNOLOGICALUNIVERSITY,BELAGAVI
B.E:Electronics & Communication Engineering NEP, OutcomeBasedEducation (OBE)and ChoiceBased CreditSystem(CBCS)
(Effectivefromthe academicyear 2022–23)

VISemester

BasicVLSIDesign			
CourseCode	**21EC654D**	CIEMarks	50
TeachingHours/Week(L:T:P:S)	3:0:0:1	SEEMarks	50
TotalHoursofPedagogy	40	TotalMarks	100
Credits	3	ExamHours	3

Courseobjectives:

- ImpartknowledgeofMOStransistortheoryandCMOStechnologies
- Impartknowledgeonarchitecturalchoicesandperformance trade-offsinvolvedindesigningandrealizingthecircuitsin CMOStechnology
- Cultivatetheconceptsofsubsystemdesignprocesses
- DemonstratetheconceptsofCMOStesting

Teaching-LearningProcess(GeneralInstructions)

Thesamplestrategies,whichtheteachercanusetoacceleratetheattainmentofthevariouscourseoutcomesare listedin thefollowing:

1. Lecturemethod(L)doesnotmeanonlythetraditionallecturemethod,butadifferenttypeofteachin gmethodmaybeadopted todevelop theoutcomes.
2. ShowVideo/animationfilmstoexplainthefunctioningofvarioustechniques.
3. Encouragecollaborative(Group)Learningintheclass
4. AskatleastthreeHOTS(Higher-orderThinking)questionsintheclass,whichpromotescriticalthinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinkingskillssuchastheabilitytoevaluate,generalize,andanalyzeinformationratherthansimplyreca llit.
6. Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeupwiththeirow ncreative ways to solvethem.
7. Discusshoweveryconceptcanbeappliedtotherealworld-andwhenthat'spossible,ithelpsimprovethe students'understanding.
8. IncorporateprogrammingexamplesgivenunderActivitybasedlearning.

Module-1

Introduction:ABrief History,MOS Transistors, MOSTransistor Theory,IdealI-V Characteristics,Non-idealI-VEffects,DCTransferCharacteristics (1.1,1.3,2.1,2.2, 2.4,2.5ofTEXT2).
Fabrication:nMOSFabrication,CMOSFabrication[P-wellprocess,N-wellprocess,Twintubprocess],BiCMOSTechnology (1.7,1.8,1.10of TEXT1).

Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2

Module-2

MOSandBiCMOSCircuitDesignProcesses:MOSLayers,StickDiagrams,DesignRulesandLayout.
BasicCircuitConcepts: SheetResistance,AreaCapacitancesofLayers,StandardUnitofCapacitance, SomeAreaCapacitanceCalculations,DelayUnit,InverterDelays,DrivingLargeCapacitiveLoads(3.1to3.3,4.1,4.3to4.8ofTEXT1).

Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Module-3	
ScalingofMOSCircuits:ScalingModels&ScalingFactorsforDeviceParameters **Subsystem Design Processes**: Some General considerations, An illustration of Design Processes,**Illustration of the Design Processes**: Regularity, Design of an ALU Subsystem, The Manchester Carry-chainandAdderEnhancementTechniques (5.1,5.2, 7.1,7.2,8.2,8.3, 8.4.1,8.4.2 ofTEXT1).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-4	
SubsystemDesign:Some ArchitecturalIssues,SwitchLogic,Gate(restoring)Logic,ParityGenerators,Multiplexers, The ProgrammableLogicArray(PLA) (6.1to6.3,6.4.1,6.4.3,6.4.6 ofTEXT1). **FPGABasedSystems**:Introduction,Basicconcepts,DigitaldesignandFPGAs,FPGAbasedSystemdesign,FPGA architecture, Physical designfor FPGAs(1.1to1.4,3.2,4.8ofTEXT3).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-5	
Memory,RegistersandAspectsofsystemTiming:SystemTimingConsiderations,SomecommonlyusedStorage/Memoryelements(9.1,9.2ofTEXT1). **Testing and Verification**: Introduction, Logic Verification, Logic Verification Principles,ManufacturingTestPrinciples,Designfortestability (12.1,12.1.1, 12.3, 12.5,12.6ofTEXT2).	
Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Courseoutcome(CourseSkillSet)

Attheendofthecoursethestudentwillbeableto:

1. DemonstrateunderstandingofMOStransistortheory,CMOSfabricationflowandtechnologyscaling.
2. Drawthebasicgatesusingthestickandlayoutdiagramswiththeknowledgeofphysicaldesignaspects.
3. InterpretMemoryelementsalongwithtimingconsiderations
4. DemonstrateknowledgeofFPGAbasedsystemdesign
5. InterprettestingandtestabilityissuesinVLSIDesign
6. AnalyzeCMOSsubsystemsandarchitecturalissueswiththedesignconstraints.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A studentshall be deemed to have satisfied the academic requirements and earned the credits allotted to eachsubject/ course if the student secures not less than 35% (18 Marks out of50) in the semester-endexamination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (ContinuousInternalEvaluation)andSEE(Semester End Examination)taken together.

ContinuousInternalEvaluation:

ThreeUnitTestseachof **20Marks(duration01hour**)

1. Firsttestattheendof5thweekofthesemester
2. Secondtestattheendofthe10thweekofthesemester
3. Third test at the end of the 15thweek of the

semesterTwo assignmentseachof**10 Marks**

4. Firstassignmentattheendof4thweek ofthesemester
5. Secondassignmentat theendof9thweekofthesemester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20Marks** (**duration01 hours**)

6. Attheendofthe13th weekofthesemester

Thesumofthreetests,twoassignments,andquiz/seminar/groupdiscussionwillbeoutof100marksandwillbe **scaled downto50marks**

(tohavelessstressedCIE,theportionofthesyllabusshouldnotbecommon/repeatedforanyofthemethodsofth eCIE.Eachmethod ofCIEshouldhaveadifferentsyllabusportionof thecourse).

CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutco me defined for thecourse.

SemesterEndExamination:

TheorySEEwillbeconductedbyUniversityasperthescheduledtimetable,withcommonquestionpapersforthes ubject(**duration 03 hours)**

1. Thequestionpaperwillhavetenquestions.Eachquestionissetfor20marks.
2. Therewillbe2questionsfromeachmodule.Eachofthetwoquestionsunderamodule(withamaximum of3sub-questions),**shouldhaveamixoftopics**underthat module.

The students have to answer 5 full questions, selecting one full question from each module.Marks scoredoutof100shallbe reducedproportionallyto50marks

SuggestedLearningResources:

TextBooks:

1. "BasicVLSIDesign"- DouglasAPucknell&KamranEshraghian,PHI,3rd Edition.
2. "CMOSVLSIDesign-ACircuitsandSystemsPerspective",NeilHEWeste,DavidHarris,AyanBanerjee,3rd Edition,PearsonEducation.
3. "FPGABasedSystemDesign",WayneWolf,PearsonEducation,2004,TechnologyandEngineering.

WeblinksandVideoLectures(e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

Wherevernecessary**Cadence/Synopsis/MentaGraphicstools**mustbeused.

1.WriteVerilogCodeforthefollowingcircuitsandtheirTestBenchforverification,observethewaveform and synthesize the code with technological library with given Constraints*. Do the initialtimingverification withgatelevel simulation.

i. Aninverter
ii. ABuffer
iii. TransmissionGate
iv. Basic/universalgates
v. Flipflop -RS,D, JK,MS, T
vi. Serial&Paralleladder
vii. 4-bitcounter[SynchronousandAsynchronouscounter]

2.Designanop-ampwithgivenspecification*usinggivendifferentialamplifierCommonsourceandCommonDrainamplifieri nlibrary**and completingthedesignflowmentionedbelow:

a. Drawtheschematicandverifythefollowing
   i) DCAnalysis
   ii) ACAnalysis
   iii) TransientAnalysis
b. DrawtheLayout andverifytheDRC,ERC
c. CheckforLVS
d. ExtractRCandbackannotatethesameandverifythe Design.

03.10.2022

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics and Communication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022-2023)

V Semester

NOTE: This Laboratory can be conducted using Industry standard EDA tool like Cadence , Synopsis or any equilent VLSI tool.

VLSI Design and Testing LAB			
Course Code	**BECL606**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

Sl.No.	Experiments
1	Design a 4-Bit Adder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALUBehavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path

	• Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
6	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
7	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increasethe drive strength to 2X and 4X and tabulate the results.

8	Construct the schematic of the Boolean Expression $Y = AB+CD+E$ using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Tabulate the results.
9	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
10	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments (For CIE)

11	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path

12	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record theobservations.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL.
2. Understand the synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
4. Design and simulate basic CMOS circuits like inverter, NOR gate and any Boolean expression .
5. Perform RTL_GDSII flow and understand the stages in ASIC design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shallbe deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubricsfor the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of thepractical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbe evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} weekof the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

03.10.2022

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.
The duration of SEE is 03 hours.
Rubrics suggested in Annexure-II of Regulation book

03.10.2022

FPGA Based System design Lab Using Verilog		Semester	VI
Course Code	**BEC657A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course objectives:

This laboratory course enables students to

- Understand FPGA Design flow for VLSI Chip Design
- Understand the concept of Design and implementation of Advanced Digital System Design
- Learning the Implementation of advanced digital circuits on FPGA boards

	Verilog Program can be compile using any compiler, Verifying the functionality using suitable simulator. Down load the programs on FPGA boards and Verify the Functionality
1	Write a Verilog description for the following combinational logic, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modelling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2	Write a Verilog description for the following Sequential Circuits,Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3	Write a Verilog description for the following Sequential Circuits, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. Ring counter
4	Write a Verilog description for the following Digital Circuits, Verify the functionality usingVerilog test bench and perform the synthesis by downloading the design on to FPGA device. a.4-Bit Ripple Carry Adder b. 4-Bit Linear Feedback shift register
5	Write a Verilog description for the following Digital Circuits, Verify the functionality using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-bitArray Multiplication b. 4-bit Booth Multiplication

6	Write a Verilog description to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality using output device.
7	Interface a Stepper motor to FPGA andWrite a Verilog description to controlStepper motor rotation.
8	Interface a DAC to FPGA and Write a Verilog descriptionto generate Squre wave of frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an output device.
9	Write a Verilog descriptionto convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.

Course outcomes:

- Familiarize with the EDA tool to write HDL programs to understand simulation and synthesis of digital design.
- Design, Simulation and Synthesis of Combinational circuits using EDA tool
- Design, Simulation and Synthesis of Sequential Circuits using EDA tool
- Interfacing DAC to FPGA device to generate different waveforms using Verilog HDL.
- Interfacing Stepper motor to FPGA device to count the number of rotations of a stepper motor.

.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1) SamirPalnitkar, "Verilog HDL : A guide to digital design and synthesis", Pearson Education, II Edition.

2) Donald E Thomas, Philip R Moorby, "The Verilog hardware description Language", Springer Science Business Media , LLC, 5th Edition

3) Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI),II Edition

4) Padmanabhan, Tripura Sunadri, "Design through Verilog HDL", Wiley, 2016.

5) Verilog HDL user manual

System Modelling using Simulink		Semester	5
Course Code	**BEC657B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination type (SEE)	**Practical**		

Course objectives:

- Understand the basics of MATLAB Simulink used for engineering applications
- Simulation of the trigonometric functions and display of signals.
- Implementations of analog and digital systems using Simulink.
- Implement digital logic circuits using Simulink and display the output.
- Simulation of the analog and digital communication systems using Simulink.

Sl.NO	Experiments
1	a) Generate the following signals using Simulink and display these signals on a single scope with separate inputs. i) sinusoidal signal, ii)square signal, iii) sawtooth signal, and iv) random signal b) Perform the following operations using simulink and display the output. i) y(t) = sin2t, ii) y(t) = $\frac{d(sin2t)}{dt}$, iii)y(t) = $\int sin2t$
2	Solve the second order differential equations shown below using Simulink and display the output. i) $\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + 5y = 1$ ii) $\frac{d^2y}{dt^2} + 3\frac{dy}{dt} + 4y = 5\cos 2t$
3	Design and realize the second order low pass and high pass RC filters using Simulink.
4	Design a BCD adder and use Simulink to simulate and verify its operation.
5	Design and Simulate the following using Simulink and verify its operation. a) 3–bit Up / Down Counter, b) 4–bit Ring Counter
6	Design and simulate the 4x1 Multiplexer and 1x4 Demultiplexer using Simulink
7	Find the step response of the following system functions given below, using Simulink. i) Continuous transfer function H(s) = $\frac{5(s+2)}{s(2s^2+4s+3)}$ ii) Discrete transfer function H(z) = $\frac{z^2-1.2z+1}{z^3-1.3z^2+z-0.2}$
8	Realize the FIR filter given by the impulse response h(n) = {0.08, 0.21,0.54, 0.86, 1, 0.86, 0.54, 0.21 0.08) using Simulink. Obtain the frequency response characteristics.

9	Simulate the Amplitude Modulation and Demodulation using Simulink. Display the output signal and its spectrum.
10	Simulate the modulation & demodulation of a random binary data stream using QPSK using Simulink. Display the output signal and its spectrum.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Create Simulink models to perform analog and digital computations.
- Implement the Combinational Digital circuits and Sequential Digital Circuit models using Simulink.
- Implement analog and digital systems using the transfer functions in s-domain and z-domain respectively.
- Demonstration of analog and digital communication modulation and demodulation using Simulink.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Steven T. Karris, "Introduction to Simulink® with Engineering Applications", Orchard Publications, 2011, ISBN : 978-1934404218
2. Devendra K. Chaturvedi, "Modeling and Simulation of Systems Using MATLAB and Simulink", CRC Press Taylor & Francis Group, 2010, ISBN 9780815351382

IoT (Internet of Things) Lab		Semester	6
Course Code	BEC657C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects.

Sl.No.	Experiments
1(i)	To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds.
1(ii)	To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2 (i)	To interface the DHT11 sensor with Arduino /Raspberry Pi and write a program to print temperature and humidity readings.
2(ii)	To interface OLED with Arduino /Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4(i)	Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.
4(ii)	Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to _thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from _thingspeak _cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.
12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the Internet of Things and its hardware and software components.
- Interface I/O devices, sensors & communication modules.
- Remotely monitor data and control devices.

- Develop real-life IoT-based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands-on Approach", University Press
- Dr. SRN Reddy, Rachit Thukral, and Manasi Mishra, "Introduction to Internet of Things: A Practical Approach", ETI Labs
- Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
- Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
- Adrian McEwen, "Designing the Internet of Things", Wiley
- Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

Python Programming for Machine Learning Applications		Semester	**6**
Course Code	BEC657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge Machine Learning Algorithms
- To develop skills required to build real-life ML Algorithm projects.

Sl.No.	Experiments
1	Solve the Tic-Tac-Toe problem using the Depth First Search technique.
2	Show that the 8-puzzle states are divided into two disjoint sets, such that any state is reachable from any other state in the same set, while no state is reachable from any state in the other set.
3	To represent and evaluate different scenarios using predicate logic and knowledge rules.
4	To apply the Find-S and Candidate Elimination algorithms to a concept learning task and compare their inductive biases and outputs.
5	To construct a decision tree using the ID3 algorithm on a simple classification dataset
6	To assess how the ID3 algorithm performs on datasets with varying characteristics and complexity, examining overfitting, underfitting, and decision tree depth.
7	To examine different types of machine learning approaches (Supervised, Unsupervised, Semi-supervised, and Reinforcement Learning) by setting up a basic classification problem and exploring how each type applies differently
8	To understand how Find-S and Candidate Elimination algorithms search through the hypothesis space in concept learning tasks, and to observe the role of inductive bias in shaping the learned concept.
9	To go through all stages of a real-life machine learning project, from data collection to model fine-tuning, using a regression dataset like the "California Housing Prices."
10	To perform binary and multiclass classification on the MNIST dataset, analyze performance metrics, and perform error analysis.
11	**Demo experiments**
12	Demo experiments

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Apply machine learning algorithms to real life problems.
- Able to make use of different machine learning approaches.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,

Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015

2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.

3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013

4. AurelienGeron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.

Microwave Engineering and Antenna Theory		Semester	7
Course Code	**BEC701**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

This course will enable students to:

1. Describe the microwave properties and its transmission media.
2. Describe the microwave devices for several applications.
3. Understand the basic concepts of antenna theory.
4. Identify antenna types for specific applications.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
3. Adopt Problem Based Learning (PBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
5. Using videos for demonstration of the fundamental principles to students for better understanding of concepts.
6. Demonstration of microwave devices and Antennas in the lab environment where students can study them in real time.

MODULE-1

Microwave Sources: Introduction, Gunn Diode (Text 2: 7.1,7.1.1,7.1.2)

Microwave transmission lines: Microwave frequencies, Microwave devices, Microwave systems. Transmission line equations and solutions, Reflection Coefficient and Transmission Coefficient. Standing wave and standing wave ratio. Smith chart, Single stub matching.

Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 (except double stub matching)

Teaching-Learning Process	Chalk and Talk would be helpful for the quantitative analysis. Videos of the Basic principles of the devices would help students to grasp better. **RBT Level**: L1, L2, L3

MODULE-2

Microwave Network Theory: Introduction, S matrix representation of multi-port networks (Text 1: 6.1, 6.3, 6.3.1, 6.3.2)

Microwave passive devices: Coaxial connectors and Adapters, Attenuators, Phase shifters, waveguide Tees, Magic Tee, Circulator, Isolator. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16, 6.4.17 A, B)

Teaching-Learning	Chalk and Talk, PowerPoint Presentation
MODULE-3	
Strip Lines: Introduction, Microstrip lines, Parallel Strip lines (Text 2: 11.1,11.2) **Antenna Basics**: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam efficiency, Directivity and Gain, Antenna Aperture Effective height, Bandwidth, Radio communication Link, Antenna Field Zones (Text 3: 2.1-2.7, 2.9-2.11, 2.13).	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3
MODULE-4	
Point sources and arrays: Introduction, Point Sources, Power patterns, Power theorem, Radiation Intensity, Arrays of 2 isotropic point sources, Pattern multiplication, Linear arrays of n Isotropic sources of equal amplitude and Spacing. (Text 3: 5.1-5.6, 5.9, 5.13) **Electric Dipole**: Introduction, Short Electric dipole, Fields of a short dipole. Radiation resistance of a short dipole. Thin linear antenna (field analysis). (Text 3: 6.1-6.5)	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3
MODULE-5	
Loop and Horn antenna: Introduction: Small loop, Comparison of far fields of small loop and short dipole. Radiation resistance of small loop, Horn Antennas, Rectangular antennas. (Text 3: 7.1,7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20) **Antenna Types**: Yagi Uda array, Parabolic Reflector, Microstrip Antennas, Features of Microstrip Antennas, (Text 3: 8.8, 9.5, 14.1,14.2)	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.
2	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench setup
3	To measure unknown impedance using Smith chart through test bench setup.
4	Study of characteristics of E plane Tee / H plane Tee.
5	Study of characteristics of Magic Tee.
6	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
7	Coupling and Isolation characteristics of microstrip directional coupler.
8	Determination of power division of microstrip power divider.
9	To plot a 2D and 3D radiation pattern of dipole Antenna (Use any simulation software)
10	Obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to transmission lines.
3. Identify microwave devices for several applications.
4. Analyze various antenna parameters and their significance in building the RF system.
5. Identify various antenna configurations for suitable applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Text Books:

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2ndEdition, 2010.
2. Microwave Devices and Circuits – Samuel Y Liao, Pearson Education.
3. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013.

Reference Books:

1. Microwave Engineering -David M Pozar, John Wiley India Pvt Ltd., Pvt Ltd., 3rd edition, 2008.
2. Microwave Engineering-Sushrut Das, Oxford Higher Education, 2nd Edn, 2015.
3. Antennas and Wave Propagation- Harish and Sachidananda, Oxford University Press, 2007.

Web links and Video Lectures (e-Resources):

1. https://www.tutorialspoint.com/antenna_theory/antenna_theory_horn.html
2. http://www.antenna-theory.com/antennas/smallLoop.php

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve practical skills

COMPUTER NETWORKS & PROTOCOLS
B.E., VII Semester, Electronics & Communication Engineering [As per Choice Based Credit System (CBCS) Scheme]

Course Code	BEC702	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

*Understand the layering architecture of OSI reference model and TCP/IP protocolsuite.

*Understand the protocols associated with each layer.
*Learn the different networking architectures and their representations.
* Learn the various routing techniques and the transport layer services.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.. Network Models: TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP(1.1,1.2, 1.3.1to 1.3.4,2.2, 2.3 ,9.1, 9.2.1, 9.2.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Data Link Control (DLC) services: Framing, Flow and Error Control. Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Connecting Devices: Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches, Advantages. Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control. (11.1,12.1,13.1, 13.2.1 to 13.2.5,15.1,17.1,17.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. IPv6 addressing and Protocol. Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. (18.1(excluding 18.1.3), 18.2, 18.4,19.1,20.1, 20.2,22.1 and 22.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol, Piggybacking Transport-Layer Protocols in the Internet: User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Error control, TCP congestion control. (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4, 23.2.5,24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.6, 24.3.8, 24.3.9)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client Server Protocols: Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. Quality of Service (25.1, 26.1.2, 26.2, 26.3, 26.6, 30.1, 30.2.)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following :

Sl.No	Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet or any other equivalent tool
1	Implement a point to point network with four nodes and duplex links between them.Analyze the network performance by setting the queue size and varying the bandwidth.
2	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3.Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine thenumber of packets sent by TCP/UDP.
3	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes andobtain congestion window for different sources/ destinations.
5	Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6	Implementation of Link state routing algorithm
Implement the following using programming languages C/C++ etc,.	
7	Write a program for a HLDC frame to perform the following. i) Bit stuffing ii) Character stuffing.
8	Write a program for distance vector algorithm to find suitable path for transmission
9	Implement Dijkstra‘s algorithm to compute the shortest routing path.
10	For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify theprogram for the cases : i)with out error ii)with error
11	Implementation of Stop and Wait Protocol and Sliding Window Protocol
12	Write a program for congestion control using leaky bucket algorithm.

Course Outcomes

At the end of the course the student will be able to:

1. Understand the concepts of networking thoroughly.
2. Identify the protocols and services of different layers.
3. Distinguish the basic network configurations and standards associated with each network.
4. Discuss and analyze the various applications that can be implemented on networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Book:

Data Communications and Networking, Forouzan, 5th Edition, McGraw Hill, 2016 ISBN: 1-25-906475-3

Reference Books:

1.A.S Tanenbaum - Computer Networks, 4th Edition, PHI, 2003
2.Computer Networks, James J Kurose, Keith W Ross, Pearson Education,2013, ISBN: 0-273-76896-4
3.Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

Wireless Communication Systems		Semester	5
Course Code	BEC703	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Understand the concepts of signal propagation over wireless channels
- Understand the multiple access techniques used in cellular communications standards.
- Understand the system architecture and layers of LTE based on the use of OFDMA and SC-FDMA principles.
- Understand the design and coding of MIMO wireless systems .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Principles of Wireless Communications: The Wireless Communication Environment, Modelling of wireless systems, System model for narrowband Signals, Rayleigh fading Wireless Channel.

The Wireless Channel: Basics of Wireless Channel Modelling, Average Delay Spread in Outdoor Cellular Channels, Coherence bandwidth, Relation between ISI and Coherence Bandwidth, Doppler fading, Doppler Impact on a wireless Channel, Coherence Time.

[**Text1:** 3.1 to 3.4, 4.1 to 4.7]

Module-2

Code Division for Multiple Access (CDMA): Basic CDMA Mechanism, Fundamentals of CDMA codes, Spreading Codes based on PN sequences, Correlation Properties of Random CDMA Spreading Sequences, Advantages of CDMA.

Orthogonal Frequency Division Multiplexing (OFDM): Introduction, Motivation and Multicarrier basics, OFDM basics, OFDM Example, MIMO OFDM, OFDM Peak to Average Power ratio, SC-FDMA.

[**Text1:** 5.1 to 5.5, 5.7, 7.1, 7.2, 7.3, 7.5, 7.7, 7.8]

Module-3

Evolution of Cellular Technologies: First Generation Cellular Systems, 2G Digital cellular systems – GSM and its Evolution, 3G Broadband Wireless Systems, Key Enabling Technologies and features of LTE, LTE Network Architecture.

Frequency Domain Multiple Accesses: Multiple Access for OFDM Systems, Orthogonal Frequency Division Multiple Access, Single Carrier Frequency Division Multiple Access.

[Text2: 1.2.1, 1.2.1.1, 1.2.2, 1.2.2.1, 1.2.3 (Only the mentioned sections and subsections), 1.4, 1.5, 4.1, 4.2, 4.3]

Module-4

Multiple Input Multiple Output Wireless Communications: Introduction to MIMO Communications, MIMO system Model, MIMO Zero Forcing Receiver, MIMO MMSE Receiver, Singular Value decomposition of MIMO Channel, SVD and MIMO capacity, Alamouti and Space-Time Codes, Nonlinear MIMO receiver: V-Blast, MIMO Beamforming.
[Text1:6.1,6.2, 6.3, 6.4, 6.5, 6.6, 6.8, 6.9, 6.10]

Module-5

Overview and Channel Structure of LTE: Radio Interface Architecture, LTE Design principles, Network Architecture, Radio Interface Protocols, Hierarchical Structure of LTE: Logical Channels, transport Channels and Physical Channels, Channel mapping, Downlink OFDMA Radio resources, Physical Resource Blocks for OFDMA, Uplink SC-FDMA Radio resources.
[**Text2:** 6.1 to 6.4]

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the wireless channel models for slow and fast fading environment.
2. Understand the different multiple access technologies used in wireless communications.
3. Understand the system architecture and the functional standard specified in LTE 4G.
4. Describe the of MIMO transmitter and receiver process using coding examples.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. Aditya K Jagannatham, "Principles of Modern Wireless Communication systems, Theory and Practice ", Mc Graw Hill Education (India) Private Limited, 2017, ISBN 978-81- 265-4231-4.
2. Arunabha Ghosh, Jun Zhang, Jeffrey G. Andrews, Rias Muhamed, "Fundamentals of LTE", Pearson India Education Services Private Limited, 2018, ISBN: 978-93-530-6239-2.

Reference Books

1. T L Singal, "Wireless Communications", Mc Graw Hill Education (India) Private Limited, 2016, ISBN:978-0-07-068178-1
2. Theodore Rappaport, Wireless Communications: Principles and Practice, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.

3. Gary Mullet, Introduction to Wireless Telecommunications Systems and Networks, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Web links and Video Lectures (e-Resources):

1. **Advanced 3G and 4G wireless Mobile Communications:**

   https://nptel.ac.in/courses/117104099

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open source software's OCTAVE or Python

Application Specific Integrated Circuit			
Course Code	**BEC714A**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03(Theory)

Course Learning objectives: This course will enable students to:

- Understand the ASIC design methodologies and programmable logic cells to implement a function on IC.
- Analyze the back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Understand performance evaluation parameters in FPGA and ASIC VLSI chip designs.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

Text 1: [1.1,1.2,1.5,2.6,2.7,2.8]

RBT Levels: L2

Module-2

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design.
Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

Text 1: [3.3,3.4,5.1,5.2,5.3,5.4]

RBT Levels: L2, L3

Module-3

Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

Text 1: [9.1,15.2, 15.3, 15.4,15.7]

RBT Levels: L2, L3

Module-4

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

Text 1: [16.1,16.2,16.3]

RBT Levels: L2, L3

Module-5

Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

Text 1: [17.1,17.2,17.3 , 17.4]

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Text Books:

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005

2. Khosrow Golshan Conexant Systems, Inc. 2007 Springer Science Business Media " Physical Design Essentials " An ASIC Design Implementation Perspective

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective" , Addison Wesley/ Pearson education 3rdedition, 2011
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
3. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**
- **Real world Problem Solving: Applying the ASIC front end and backend concepts.**

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl.No	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort	L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition , routing using algorithms and EDA tools	L3,L4
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L3 ,L4

B. E. Electronics and Communication Engineering
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

Computer and Network Security

Course Code	BEC714B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100

CREDITS – 03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services, Vulnerabilities in the host machines.
- Core Competence: To equip students with a basic foundation on computer as well as network security by delivering the basics of malicious software, intrusion detection, vulnerability Analysis, auditing as well as securities related to network, system, user and programs

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1	RBTL Level
Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. **(Text2: Chapter1)** Security Mechanisms, Services and Attacks, A model for Network security **(Text1: Chapter1: 3, 4, 5, 6)**	L1, L2, L3
MODULE-2	
Malicious Logic: Introduction, Trojan Horses, Computer Viruses, Computer Worms, Other Forms of Malicious Logic, Defenses (Text 3: Chapter 12) **Vulnerability Analysis:** Introduction, Penetration Studies, Vulnerability Classification, Frameworks (Text 3: Chapter 13)	L1, L2, L3
MODULE-3	

Auditing: Definitions, Anatomy of an Auditing System, Designing an Auditing System, A Posterior Design, Auditing Mechanisms, Examples, Audit Browsing (Text 3: Chapter 14) **Intrusion Detection**: Principles, Basic Intrusion Detection, Models, Architecture, Organization of Intrusion Detection Systems, Intrusion Response (Text 3: Chapter 15)	L1, L2, L3
MODULE-4	
Network Security: Introduction, Policy Development, Network Organization, Availability and Network Flooding, Anticipating Attacks (Text 3: Chapter 16) **System Security:** Introduction, Policy, Networks, Users, Authentication, Processes, Files, Retrospective (Text 3: Chapter 17)	L1, L2, L3
MODULE-5	
User Security: Policy, Access, Files and Devices, Processes, Electronic Communications (Text 3: Chapter 18) **Program Security:** Introduction, Requirements and Policy, Design, Refinement and Implementations (Text 3: Chapter 19: Section 1, 2, 3, 4)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the various types of attacks on computer and network security from malicious logic and intruders.
- Explain how to analyze the various vulnerabilities in the system which can compromise the security.
- Explain how auditing is essential to detect intrusion or suspicious activities in the system.
- Explain the process involved to provide security with respect to network, system, user and program.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.
3. Matt Bishop, Sathyanarayana S Venkatramanayya, "Introduction to Computer Security", Pearson Education, 2006, ISBN 81-7758-425-1

Reference Books

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

Automotive Electronics		Semester	7
Course Code	**BEC714C**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features
- Design and implement the electronics that attribute the reliability, safety, and smartness to automobile, providing add – on comforts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain the functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' analytical skills and develops design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to devise creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive systems, The Engine- Engine Block, Cylinder Head, four stroke Cycle, Engine Control, Ignition System- Spark plug, High voltage circuit and distribution, spark pulse generation, ignition timing, diesel engine, Drive Train – Transmission, drive shaft, differential, suspension, brakes, steering system, starter battery-operating principle. **(Text1: Chapter1, Text 2: Pg. 407-410)**

The Basics of Electronic Engine Control - Motivation for Electronic Engine, control – exhaust emissions, fuel economy, concept of an electronic engine, control system, definition of general terms, definition of engine performance terms, engine mapping, effect of air/fuel ration, spark timing and EGR on performance, control strategy, electronic fuel control system, analysis of intake manifold pressure, electronic ignition. **(Text1: Chapter 5)**

Module-2
Automotive Sensors – Automotive control system applications of sensors and Actuators – Variables to be measured, airflow rate sensor, strain gauge MAP sensor, Hall Effect position sensor, Magnetic Reluctance Crankshaft position sensor, Throttle angle sensor, Engine coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2 /EGO) Lambda sensors, piezoelectric Knock sensor **(Text 1: Chapter 6)** **Automotive Engine Control Actuators** – Solenide, Fuel Injector, EGR actuator, Ignition system **(Text 1: Chapter 6)**
Module-3
Digital Engine Control System- Digital Engine control features, Control modes for fuel control (Seven Modes), EGR Control, Electronic Ignition control- closed loop ignition timing, spark advance correction scheme, Integrated engine control system- secondary air management, Evaporative Emissions, Canister Purge, automatic system adjustment, system diagnostics **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data Processing, Programming, Digital modules in the Control Unit, Control Unit Software **(Text 2: Pg. 196-207)**

Module-4
Automotive Networking – Bus Stem- classification, Applications in the Vehicle, Coupling of networks, Examples of Networked Vehicles **(Text 2: Pg. 85-91),** **Buses** – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces **(Text 2: Pg. 92-151)** **Vehicle Motion Control –** Typical Cruise control system, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Cruse Control Configuration, Cruise Control Electronics (Digital Only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**
Module-5
Automotive Diagnostics – Timing Light, Engine Analyzer, On-Board diagnostics, Off-Board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag Systems **(Text1: Chapter10)** **Future Automotive Electronic Systems –** Alternative Fuel Engines, Electric and Hybrid Vehicles, Fuel Cell Power Cars, Collision Avoidance Radar Warning Systems, Low tire pressure warning systems, Head Up Display, Speech Synthesis, Navigation- Navigation Sensors – Radio Navigation, Signpost Navigation, Dead reckoning navigation, Voice Recognition Cell phone Dialing, Advanced Cruise Control, Stability Augmentation, Automatic Driving Control **(Text 1: Chapter 11)**
Course Outcome (Course Skill Set) At the end of the course, students will be able to: • Describe the basics of Automobile dynamics and design electronics. • Acquire an overview of automotive components, subsystems and basics of Electronic Engine Control in today's automotive industry. • Use available automotive sensors and actuators while interfacing with microcontrollers/microprocessors during automotive system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. **William B Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.**
2. **Robert Bosch GmbH (Ed.), "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", 5th edition, John Wiley & Sons Inc., 2007.**

Web links and Video Lectures (e-Resources):
Related NPTEL Courses

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving using group discussion.
- Present animation for Car assembly
- Real world example of Automotive Electronics concepts.

	Radar Communication	Semester	5
Course Code	BEC714D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives: This Course will enable the students to

- Understand the concepts of Radar, types of Radar and Applications.
- Understand the various measurements in Radar and Propagation of waves.
- Understand the various types of Radar and its functions.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to RADAR: Basic Radar, Simple Radar equation, Radar Block diagram, Radar Frequencies, Applications of Radar.

The RADAR Equation: Detection of signals in Noise, Receiver Noise and SNR, Integration of Radar Pulses, Radar Cross section of Targets, Radar Cross section Fluctuations, Transmitter Power, Pulse Repetition Frequency, Antenna parameters, System Losses.

[**Text1:** 1.1 to 1.5, 2.2, 2.3, 2.6 to 2.12]

Module-2

MTI and Pulse Doppler Radar: Introduction to Doppler and MTI Radar, Delay-Line Cancelers, Moving Target Detector, Pulse Doppler radar.

Tracking Radar: Tracking with Radar, Mono-pulse tracking, Conical Scanning and Sequential Lobing, Tracking in Range, Comparison of Trackers.

[**Text1:** 3.1, 3.2, 3.6, 3.9, 4.1, 4.2, 4.3, 4.6, 4.8]

Module-3

Information from Radar Signals: Introduction, Basic Radar Measurements, Accuracy of measurements.

Radar Clutter: Introduction, Surface-Clutter Radar equation, Land clutter sea Clutter.

Propagation of Radar Waves: Introduction, Scattering from Flat Earth, Scattering from the Round Earth's Surface, Atmospheric Refraction.

[Text1: 6.1, 6.2, 6.3, 7.1 to 7.4, 8.1 to 8.4.]

Module-4

Radar Transmitters: Introduction, Linear beam power tubes, solid state RF power sources.
Radar Receiver: Fundamentals, Receiver Noise Figure, Super heterodyne receiver, Duplexer.
[Text1: 10.1, 10.2, 10.3, 11.1 to 11.4]

Module-5

Synthetic Aperture Radar (SAR): Introduction, SAR History, General Description – Resolution, SAR Signal processing, Radar Equation of the SAR system, SAR system Design considerations.
Over-the-Horizon Radar (OTHR): Introduction, Classification, Ionospheric effects, Ray path trajectories, Principles of OTHR systems.
Secondary Surveillance Radar: Introduction, Principles of SSR, Deficiencies in SSR, Solution to deficiencies, Range performance in SSR.
[**Text-2:** 9.1 to 9.6, 14.3 to 14.6, 15.1 to 15.5]

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the principles of Radar.
2. Analyze the tracking in radar and modelling of Radars.
3. Analyze the limitations, interference and propagation of Radar waves.
4. Describe the Radar transmitter and receiver, and modern Radars.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Merrill L. Skolnik, "Introduction to RADAAR Systems", 3rd edition, Mc Graw Hill Education (India) Private Limited, 2016 (Reprint), ISBN 978-0-07-044533-8.
2. Habibur Rahman, "Fundamental Principles of RADAR", CRC Press, 2019, ISBN: 978-1-138-38779-9.

Reference Books

1. Mark A Richards, James A. Scheer, William A. Holm, "Principles of Modern RADAR", Yesdee Publishing Private Ltd, , 2012, ISBN: 978-93-80381-29-9.
2. Bassem R. Mahafza, " Radar Systems Analysis and Design using MATLAB", 4th edition, CRC press, 2022, ISBN 978-0-367-50793-0.
3. J.C. Toomay, Paul J. Hannen; "Principles of Radar", Third Edition, PHI Learning Pvt Ltd., 2011, ISBN : 978-81-203-4155-9.

Web links and Video Lectures (e-Resources):

1. **NPTEL : Radar Principles**

   https://archive.nptel.ac.in/courses/108/105/108105154/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open source software's OCTAVE or Python
2. Experiential Learning / Simulation using MATLAB.

E-Waste Management		Semester	7
Course Code	**BEC 755A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- **Understanding e-waste**: To learn about e-waste, its different types, and how it's generated
- **E-waste rules and directives**: To understand the rules and directives for e-waste in different countries
- **E-waste management**: To learn how to manage e-waste throughout its life cycle
- **Environmental and health impacts**: To understand the environmental and health impacts of e-waste

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Preamble, What is e-waste, E-waste Sources and generation, Growth of Electrical and Electronics Industry in India, Global Context of e-waste Management, Indian Scenario on e-waste Management,

E-WASTE: E-waste Definition, Classification of e-waste, Characterization of e-waste

Text 1: Chapter 1 & 2

Module-2

Regulatory Framework: Global e-waste Regulations, Waste Electronics and Electrical Equipment (WEEE Directive 82), International norms – Basel Convention, Evolution of e-waste regulations in India, E-waste Management Rules 2016 (amendments to 2011 Rules), Regulatory Compliance Mechanisms, E-waste Management Guidelines (Text 1: 3.1 to 3.7)

Module-3

Extended Producer Responsibility (EPR): E-waste – A post Consumer Waste, E-waste value Chain, E-waste Collection Systems, Extended Producer Responsibility (EPR), Collective Responsibility, Producer Responsible Organization (PRO) (Text 2: 4.1 to 4.6)

Module-4

E-Waste Handling: Characterization & Classification, Packaging and Labelling, Transportation, Storage, Safety in Handling – Precautionary Principles: Text 1- Chapter 5

Module-5

Restrictions on Use of Hazardous Substances (ROHS): Hazardous substances in e-waste, Global ROHS compliances (ROHS Directive 84), ROHS compliance requirements in India: Text 1: Chapter 6

E-Waste Recycling: E-waste Recycling Operations, Dismantling & Segregation, Recycling & Recovery, Recycling Technologies – Text 1: Chapter 7 (7.1 to 7.4)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the environmental impacts of e-waste
2. Distinguish the role of various national and internal act and laws applicable for e-waste management and handling
3. Analyse the e-waste handling methods & restrictions
4. Analyze the e-waste recycling techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. Lakshmi Raghupathy, Introduction to E-Waste Management, TERI Press, New Delhi

Reference Books:

1. Johri R., E-waste: implications, regulations, and management in India and current global best practices, TERI Press, New Delhi

Web links and Video Lectures (e-Resources):

- https://news.mit.edu/2013/ewaste-mit

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for the generated e-waste and its management and prepare a report
- Field visit to explore the possibility of various e-waste management techniques

Automotive Engineering		Semester	7
Course Code	**BEC755B**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features
- Design and implement the electronics that attribute the reliability, safety, and smartness to automobile, providing add – on comforts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain the functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' analytical skills and develops design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to devise creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive systems, The Engine- Engine Block, Cylinder Head, four stroke Cycle, Engine Control, Ignition System- Spark plug, High voltage circuit and distribution, spark pulse generation, ignition timing, diesel engine, Drive Train – Transmission, drive shaft, differential, suspension, brakes, steering system, starter battery-operating principle. **(Text1: Chapter1, Text 2: Pg. 407-410)**

The Basics of Electronic Engine Control - Motivation for Electronic Engine, control – exhaust emissions, fuel economy, concept of an electronic engine, control system, definition of general terms, definition of engine performance terms, engine mapping, effect of air/fuel ration, spark timing and EGR on performance, control strategy, electronic fuel control system, analysis of intake manifold pressure, electronic ignition. **(Text1: Chapter 5)**

Module-2
Automotive Sensors – Automotive control system applications of sensors and Actuators – Variables to be measured, airflow rate sensor, strain gauge MAP sensor, Hall Effect position sensor, Magnetic Reluctance Crankshaft position sensor, Throttle angle sensor, Engine coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2 /EGO) Lambda sensors, piezoelectric Knock sensor **(Text 1: Chapter 6)** **Automotive Engine Control Actuators** – Solenide, Fuel Injector, EGR actuator, Ignition system **(Text 1: Chapter 6)**
Module-3
Digital Engine Control System- Digital Engine control features, Control modes for fuel control (Seven Modes), EGR Control, Electronic Ignition control- closed loop ignition timing, spark advance correction scheme, Integrated engine control system- secondary air management, Evaporative Emissions, Canister Purge, automatic system adjustment, system diagnostics **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data Processing, Programming, Digital modules in the Control Unit, Control Unit Software **(Text 2: Pg. 196-207)**

Module-4

Automotive Networking – Bus Stem- classification, Applications in the Vehicle, Coupling of networks, Examples of Networked Vehicles **(Text 2: Pg. 85-91),**
Buses – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces **(Text 2: Pg. 92-151)**

Vehicle Motion Control – Typical Cruise control system, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Cruise Control Configuration, Cruise Control Electronics (Digital Only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**

Module-5

Automotive Diagnostics – Timing Light, Engine Analyzer, On-Board diagnostics, Off-Board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag Systems **(Text1: Chapter10)**

Future Automotive Electronic Systems – Alternative Fuel Engines, Electric and Hybrid Vehicles, Fuel Cell Power Cars, Collision Avoidance Radar Warning Systems, Low tire pressure warning systems, Head Up Display, Speech Synthesis, Navigation- Navigation Sensors – Radio Navigation, Signpost Navigation, Dead reckoning navigation, Voice Recognition Cell phone Dialing, Advanced Cruise Control, Stability Augmentation, Automatic Driving Control **(Text 1: Chapter 11)**

Course Outcome (Course Skill Set)

At the end of the course, students will be able to:

- Describe the basics of Automobile dynamics and design electronics.
- Acquire an overview of automotive components, subsystems and basics of Electronic Engine Control in today's automotive industry.
- Use available automotive sensors and actuators while interfacing with microcontrollers/microprocessors during automotive system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. **William B Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.**
2. **Robert Bosch GmbH (Ed.), "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", 5th edition, John Wiley & Sons Inc., 2007.**

Web links and Video Lectures (e-Resources):
Related NPTEL Courses

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving using group discussion.
- Present animation for Car assembly
- Real world example of Automotive Electronics concepts.

	Embedded Systems Applications		Semester	7
	Course Code	**BTE755C**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- Understand the fundamental concepts, characteristics, and applications of embedded systems across various domains.
- Analyse the hardware components of embedded systems, including microcontrollers, memory, and low-power design techniques.
- Explore the role of sensors, ADCs, and actuators in embedded systems, and their interfacing with digital systems.
- Apply embedded systems design principles in real-world applications such as mobile phones, automotive electronics, RFID, and biomedical systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to embedded systems: Application domain of embedded systems, desirable features and general characteristics of embedded systems, model of an embedded system, microprocessor Vs microcontroller, example of a simple embedded system, figure of merit for an embedded system, classification of MCUs: 4/8/16/32 bits, history of embedded systems, current trends.

(Text: 1.1 to 1.9)

Module-2

Embedded systems-The hardware point of view: Microcontroller unit (MCU), The Processor, The Harvard Architecture, A popular 8-bit MCU: General Purpose I/O (GPIO), Clock; Memory for embedded systems: Semiconductor Memory, Random Access Memory (RAM), Static RAM (SRAM), An SRAM Chip. Low Power Design, Pull up and Pull Down Resistors.

(Text: 2.1 to 2.2.2, 2.3 to 2.3.2.2 and 2.4 to 2.5)

Module-3

Sensors, ADCs and Actuators

Sensors: Temperature Sensor, Light Sensor, Proximity/range Sensor; Analog to digital converters: ADC Interfacing, Control Interface, Data Interface; Actuators: Displays, Light Emitting Diodes (LED), Seven Segment LED; Motors: Stepper Motors, DC Motors.

(Text: 3.1.1 to 3.1.3, 3.2 to 3.2.1.2, 3.3 to 3.3.1.2 and 3.3.2 to 3.3.2.2)

Module-4

	Examples of embedded systems: Mobile phone, Automotive electronics, Radio Frequency Identification (RFID), Wireless Sensor Networks (WISENET), Robotics, Biomedical applications, Brain machine interface. (Text: 4.1 to 4.7)
	Module-5
	Embedded Design-A Systems Perspective: A Typical Example, Product Design, The Design Process, Testing, Bulk Manufacturing. (Text: 18.1 to 18.5)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the fundamental concepts and characteristics of embedded systems, including their classification and modern trends.
2. Analyse the architecture and hardware components of MCUs and their role in embedded systems.
3. Apply knowledge of sensors, ADCs, and actuators for interfacing and control in embedded systems.
4. Evaluate real-world embedded system applications such as mobile phones, automotive electronics, RFID, and robotics.
5. Develop an understanding of the embedded design process, from concept to bulk manufacturing, including testing and product design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Das, LyLa B.. Embedded Systems: An Integrated Approach. India: Pearson Education India, ISBN 9788131787663, 2013.

Web links and Video Lectures (e-Resources):

- Embedded Systems: https://nptel.ac.in/courses/108102045
- Embedded Systems Design: https://onlinecourses.nptel.ac.in/noc20_cs14/preview
- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Students can interface a temperature sensor with an ADC and display the digital output on a seven-segment display, demonstrating sensor integration with actuators.

	Sensors and Actuators	Semester	7
Course Code	**BEC755D**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- To provide the fundamental knowledge about sensors and measurement system.
- To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.
- To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.
- To discuss basics of signal conditioning and signal conditioning equipment.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical Thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Sensors and Transducers: Introduction, Definition of Sensors and Transducers, Classification of Transducers, Advantages and Disadvantages of Electrical Transducers. **(Text 1:16.1 to 16.4)**

Measurement: Introduction to measurement and Instrumentation, Definition, significance of Measurement, Methods of measurement, Modes of measurement, Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, Applications of measurement systems. **(Text 1:3.1 to 3.7)**

Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation. **RBT Level:** L1, L2, L3

Module-2

Static and Dynamic Characteristics of instruments: Introduction, Definition relating to measuring instruments.

Static characteristics - Accuracy, Errors and Correction, Static calibration Range and span. Scale readability Repeatability and Reproducibility, Drift, Accuracy and Precision, Sensitivity, Linearity, Hysteresis, Threshold and Resolution, Dead Zone and Dead Time, Loading Effects and Noise.

Dynamic Characteristics– Dynamic Response, Dynamic characteristics of a measurement system, Dynamic analysis of a measurement system, Zero, First and Second order system.

(Text 1: 3.8, 3.8.1 to 3.8.4.4)

Teaching-Learning Process	Chalk and Talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Measurement of Temperature: Introduction, Temperature measuring instruments, RTD, Thermistors, Thermocouple Thermometers, Radiation Pyrometers, Optical Pyrometers. **(Text 1: 21.2, 21.2.1 to 21.2.7)** **Measurement of Displacement:** Introduction, Principles of Transduction –Variable resistance devices, Variable Inductance Transducer, Induction Potentiometers, Synchros and Resolvers, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer. **(Text 2: 4, 4.1 to 4.3)**	
Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors **RBT Level:** L1, L2, L3
Module-4	
Measurement of Strain: Introduction, Factors affecting strain measurements, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges, Thin film Guages (principle, types & list of characteristics only), Strain gauge Circuits – Wheatstone bride circuit, Applications. **(Text 2: 5, 5.1 to 5.5, 5.8, 5.8.1, 5.10)** **Measurement of Force & Torque:** Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. **Torque measurement:** Absorption type, transmission type, stress type & deflection type. **(Text 2: 10.1,10.2,10.2.1,10.2.2,10.2.3,10.2.6,10.7,10.8,10.9)**	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors **RBT Level:** L1, L2, L3
Module-5	
Signal Condition: Introduction, Functions of Signal Conditioning Equipment, Amplification, Types of Amplifiers, Mechanical Amplifiers Fluid Amplifiers, Optical Amplifiers, Electrical and electronic Amplifiers. **(Text 1: 17.1 to 17.8)** **Data Acquisition Systems and Conversion:** Introduction, Objectives and Configuration of Data Acquisition System, Data Acquisition Systems, Data Conversion. **(Text 1: 18.1 to 18.4)**	
Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system.
2. Interpret and analyse the static and dynamic characteristics of instruments.
3. Elucidate the working principle and usage of different transducers for temperature, and displacement measurement.
4. Discuss the principle and working of strain, force and torque measurement.
5. Analyze the signal conditioning and signal conditioning equipment.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(To have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Electrical and Electronic Measurements and instrumentation, R.K Rajput, S. Chand, 4th Edition, 2015.
2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2nd Edition (32 Reprint), McGraw Hill Education (India), 2014.

Reference Books :

1. Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17th Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004.
2. A Course in Electronics and Electrical Measurements and Instruments, J.B. Gupta, Katson Books, 13th Edition, 2008.