ACS College of Engineering
Approved by AICTE New Delhi, Affiliated to VTU, Belagavi
(A Unit of RajaRajeswari Group of Institutions)

NAAC 'A' Accredited

Department of Electronics and Communication Engineering

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY MANUAL

Subject Code: 18ECL37

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ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY
SEMESTER – III (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Laboratory Code	**18ECL37**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to

- Understand the circuit schematic and its working
- Study the characteristics of different electronic devices
- Design and test simple electronic circuits as per the specifications using discrete electronic components.
- Familiarize with EDA software which can be used for electronic circuit simulation.

Laboratory Experiments

PART A : Experiments using Discrete components

1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative)
2. Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor
3. Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation
4. Characteristics of LDR and Photo diode and turn on an LED using LDR
5. Static characteristics of SCR.
6. SCR Controlled HWR and FWR using RC triggering circuit
7. Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge.
8. Measurement of Resistance using Wheatstone and Kelvin's bridge.

PART-B : Simulation using EDA software
(EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any equivalent tool)

1. Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
2. Transfer and drain characteristics of a JFET and MOSFET.
3. UJT triggering circuit for Controller Rectifiers.
4. Design and simulation of Regulated power supply.

COURSE OUTCOME		
COs	**Electronic Devices and Instrumentation Lab (18ECL37)**	**Bloom's Level**
CO1	Understand the characteristics of various electronic devices and measurement of parameters.	**L1, L2, L3**
CO2	Design and test simple electronic circuits	**L1, L2, L3**
CO3	Use of circuit simulation software for the implementation and characterization of electronic circuits and devices	**L1, L2, L3**

INDEX

Experiment No.1
Diode Clipping and Clamping Circuits

AIM: To conduct an experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).

COMPONENTS REQUIRED:

S.N	Particulars	Type	Range	Quantity
1.	Signal Generator	---	---	01
2.	Regulated Power Supply	---	0-30V	02
3.	Oscilloscope	---	---	01
4.	Bread Board/Spring Board	---	---	01
5.	Diode	IN4007	---	02
6.	Resistor	Carbon	10KΩ	02
7.	Capacitor	Electrolyte	---	01
8.	Connecting wires	Single strand	---	few

THEORY:

The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a clipping circuit.

Clippers find extensive use in radar, digital and other electronic systems, although several clipping circuit have been developed to change the wave shape, we shall confine our attention to diode clippers. These clippers can remove signal voltages above or below a specified level

The important diode clippers are:

1. Parallel clipper circuits
2. Series clipper circuits

Further it can also be classified into:

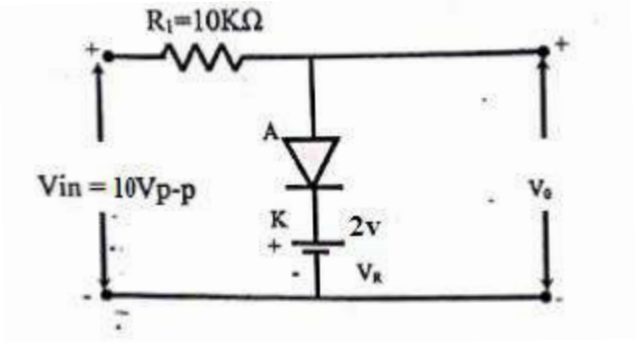
1. Positive clippers,
2. Negative clippers
3. Biased clipper
4. Combinational clippers.

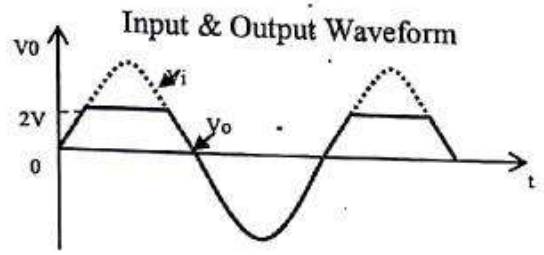
A clipping circuit comprises of linear elements like resistors and nonlinear elements like junction diode or transistor, but it does not contain energy storage elements like capacitors.
Clipping circuits are used to select, for purposes of transmission, that part of a signal wave from which lies above or below a certain reference voltage level. There are generally two categories of clippers: series and parallel. The series configuration is defined as one where diode is in series with the load while the parallel variety has the diode in a branch parallel to the load.

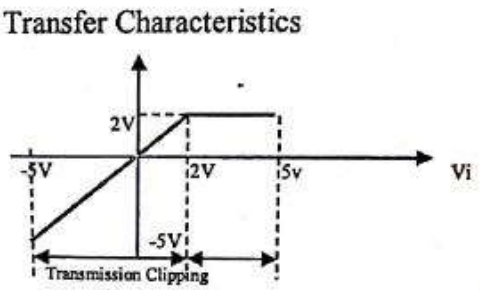
A transfer characteristic is the plot of output voltage $V_o$vs V_i that depends upon whether diode is ON or OFF. By the switching action of nonlinear element, definite relationship can be obtained between V_o and V_i in practical clipper circuits. The equation connecting V_o and V_i, is termed as transfer characteristic equation.

CIRCUIT DIAGRAM

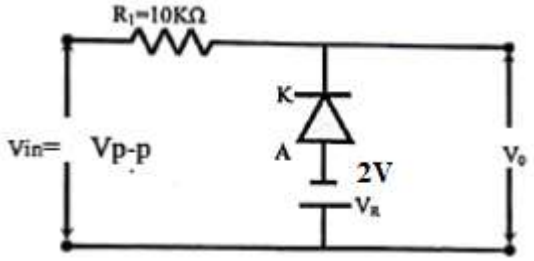
i) Positive Peak Clipping:

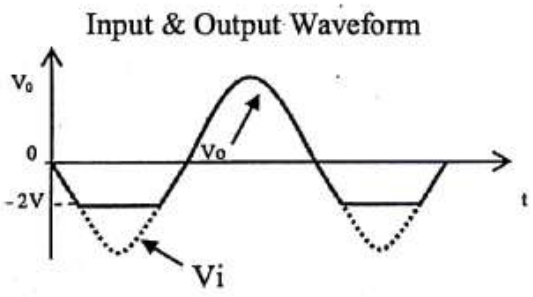


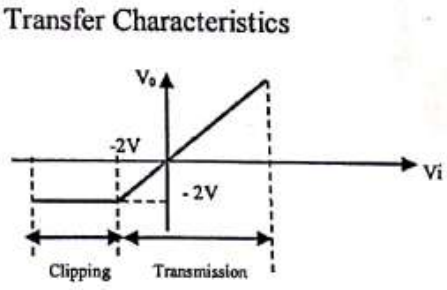




ii) Negative Peak Clipping

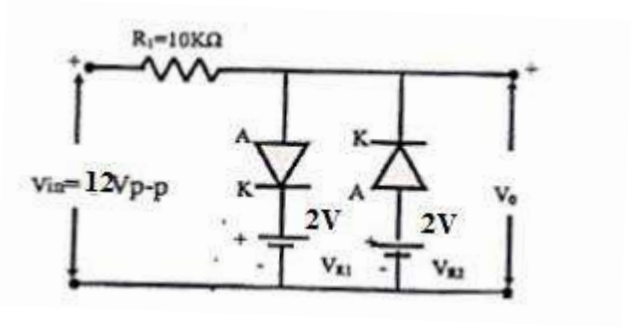


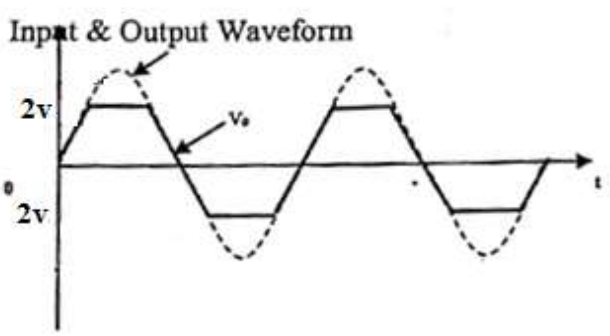


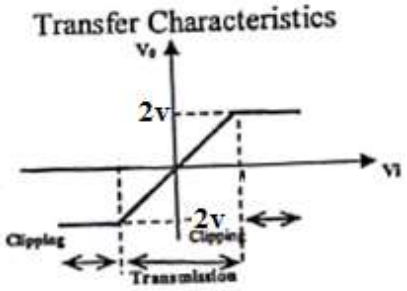


iii) Double Ended Clipping

CIRCUIT DIAGRAM:







PROCEDURE

1. Connect the components as shown in circuit diagram.
2. Apply sine wave input signal (V_i) at frequency of 1KHz from the signal generator and adjust the peak to peak amplitude 10 Vp-p.
3. Connect the input signal to channel 1, clipped output signal to channel 2 and observe input and output waveforms for different values of V_R on Oscilloscope.
4. Keep Oscilloscope in X-Y mode and observe the transfer characteristics.
5. Draw the input, output waveform and Transfer characteristics curve on the graph sheet

TABULAR COLUMN

i) Positive Peak Clipping

SL No.	Theoretical			Practical
	V_R	V_D	$V_O=V_R+V_D$	V_O
1				
2				
3				
4				
5				

ii) Negative Peak Clipping

SL No.	Theoretical			Practical
	V_R	V_D	$V_O=V_R+V_D$	V_O
1				
2				
3				
4				
5				

iii) Double Ended Clipping

SL No.	Theoretical					Practical	
	V_D	V_{R1}	V_{R2}	$V_{O1}=V_{R1}+V_D$	$V_{O2}=V_{R2}+V_D$	$V_{O1}=V_{R1}+V_D$	$V_{O2}=V_{R2}+V_D$
1							
2							
3							
4							
5							

CLAMPING CIRCUITS THEORY:

Sometimes it is necessary to add a DC level to the AC output signal. The circuits which are used to add a DC level as per the requirements to the AC output signal are called Clamper circuit. The capacitor, diode and resistance are the three basic elements of a clamper circuit. The clamper circuits are also called DC Restorer or DC Inverter circuits. Depending upon the whether the positive DC or negative DC shift is introduced in the output waveform, the clampers are classified as,

- Negative Clampers
- Positive Clampers

1. NEGATIVE CLAMPER:

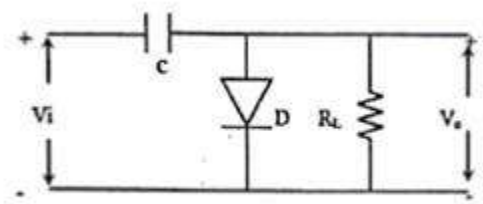


Fig:1

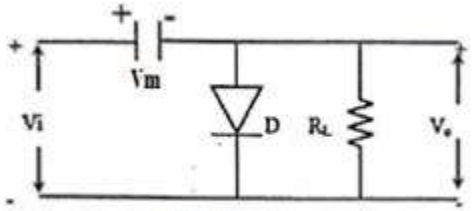


Fig:2

A simple negative clamper which adds a negative level to the AC output is shown in fig.1. It consists of a capacitor C, the ideal diode D and the load resistor R_L.

During the first positive cycle of the input voltage V_i the capacitor gets charged through forward biased diode D up to the maximum value V_m of the input signal V_i. The capacitor charging is almost instantaneous, which is possible by selecting proper values of C and R_L in the circuit. The capacitor once charged to V_m, acts as a battery of voltage V_m as shown in the fig.2.

Thus when $V_i = V_m$. the output voltage V_o is zero. As input voltage decreases after attaining its maximum value V_m, the capacitor remains charged to V_m, and the diode D becomes reverse biased. And the output voltage Vo is now given by,

$V_o = V_i - V_m$

In the negative half cycle of V_i, the diode will remains reverse biased. The capacitor starts discharging through the resistance R_L. As the time constant R_LC is very large, it can be approximated that the capacitor holds all its charge and remains charged to V_m, during this period. Hence we can write again that,

$V_o = V_i - V_m$
$V_o = -V_m$ for $V_i = 0$
$V_o = 0$ for $V_i = V_m$
$V_o = -2V_m$ for $V_i = -V_m$

2. POSITIVE CLAMPER

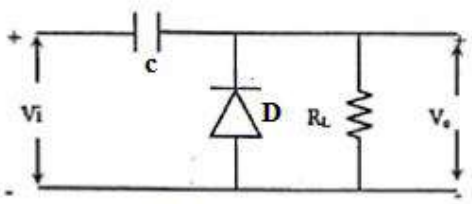


Fig:3

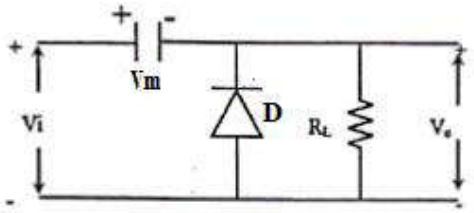


Fig:4

By changing the orientation of the diode in the negative clamper, the positive clamper circuit can be achieved. The circuit is shown in fig 3.

During the negative half cycle of the input voltage V_i, diode D gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value V_m of the input signal V_i.

The capacitor once charged to V_m, acts as a battery of voltage V_m, with the polarities as shown in fig. 4.

Thus when $V_i = V_m$, the output voltage V_o is $2V_m$. Under steady state conditions we can write,

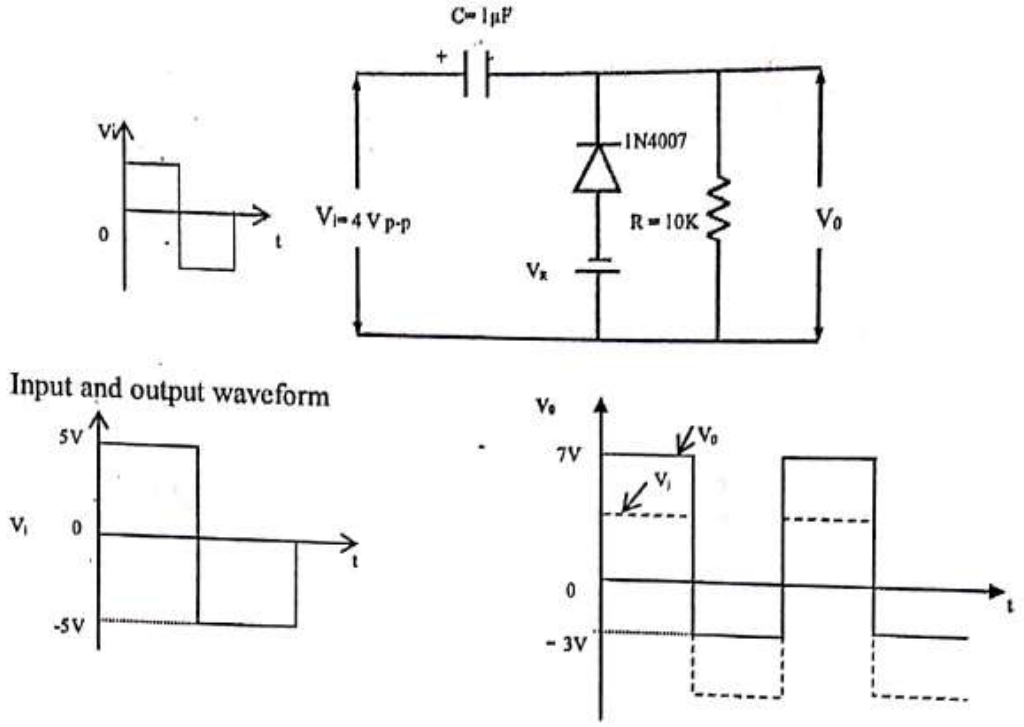
$$V_o = V_i + V_m.$$

In the positive half cycle, the diode D is reverse biased. The capacitor starts discharging through R_L But due to large time constant, it hardly gets discharged during positive half cycle of V_i. It holds its entire charge. Hence,

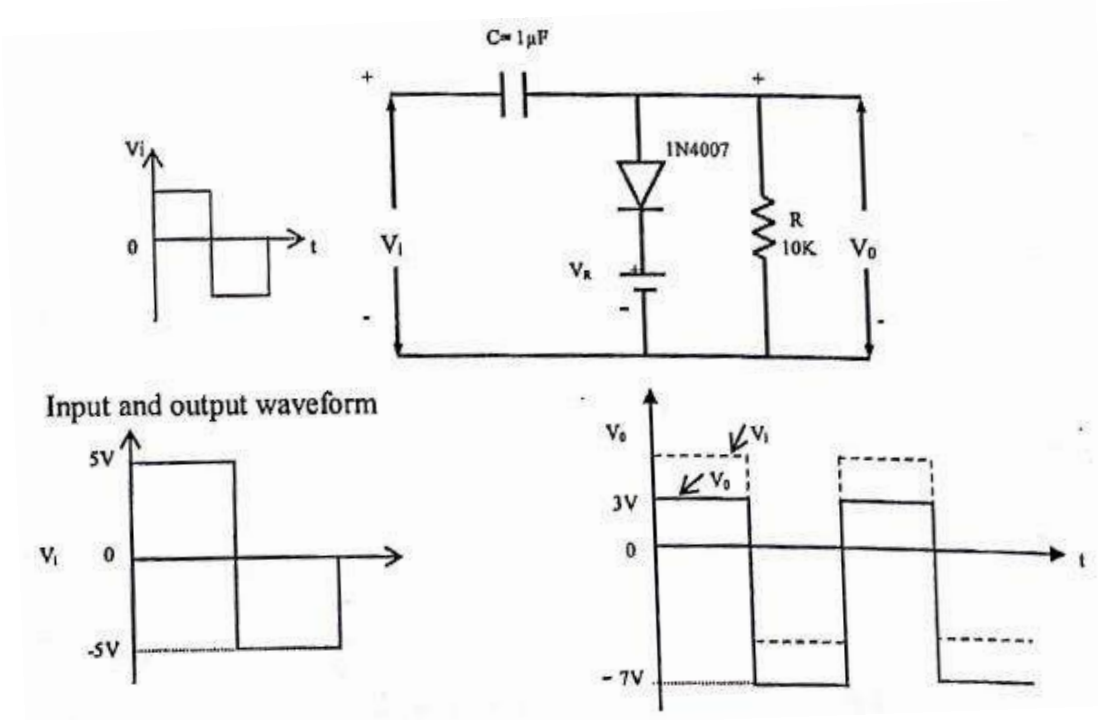
$V_o = V_i + V_m$
$V_o = V_m$ for $V_i = 0$
$V_o = 2V_m$ for $V_i = V_m$
$V_o = 0$ for $V_i = -V_m$

CIRCUIT DIAGRAM

iv) Positive Clamper:



iv) Negative Clamper:



PROCEDURE:

1. Connect the components as shown in circuit diagram.
2. Apply sine wave input signal (V_i) at frequency of KHz from the signal generator and adjust the peak to peak amplitude $4V_{p-p}$.
3. Connect the input signal to channel 1, clamped output signal to channel 2 and observe input and output waveforms for different values of V_R on Oscilloscope.
4. Draw the input and output waveform on the graph sheet.

Tabular column

i) Positive Clamper

SL. NO	Theoretical				Practical	
	V_R	V_D	$V_{o+}=V_{inp-p} - (V_R+V_D)$	$V_{o-}= -(V_R+V_D)$	V_{o+}	V_{o-}
1						
2						
3						
4						
5						

ii) Negative Clamper

SL. NO	Theoretical				Practical	
	V_R	V_D	$V_{o+}= (V_R+V_D)$	$V_{o-}= [V_{inp-p} -(V_R+V_D)]$	V_{o+}	V_{o-}
1						
2						
3						
4						
5						

Experiment No.2
Rectifier Circuits

AIM: To Design and set up half wave and full wave rectifiers with and without filters and determine ripple factor and efficiency:

COMPONENTS REQUIRED:

S.N	Particulars	Type	Range	Quantity
1.	Oscilloscope	---	---	01
2.	Bread Board	---	---	01
3.	Diode	IN4007	---	02
4.	Resistor	Carbon	10KΩ	01
5.	Capacitor	Electrolyte	10µF	01
6.	Transformer		12-0-12Vpp	01
7.	Connecting wires	Single strand	---	few

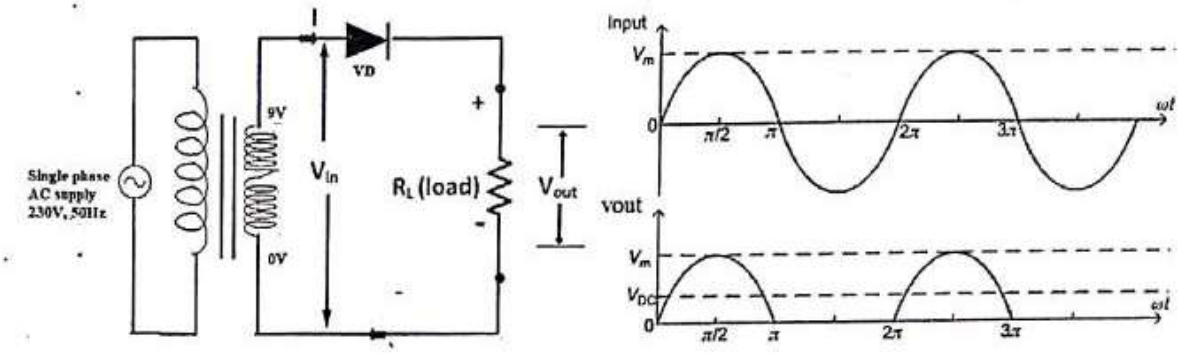
THEORY:

Rectification is the process of converting the alternating quantity (AC) to the unidirectional quantity (DC with pulsation). The transformer is used to step down the voltage from 230V to the desired level. Then, the diode is responsible for the conversion of ac available at the secondary of the transformer into DC with pulsation. Hence, the diode used for this application is also referred as rectifier. The capacitor connected across the load (resistor) is behaving as a filter. Filter is responsible to smooth the pulsating DC into pure DC.

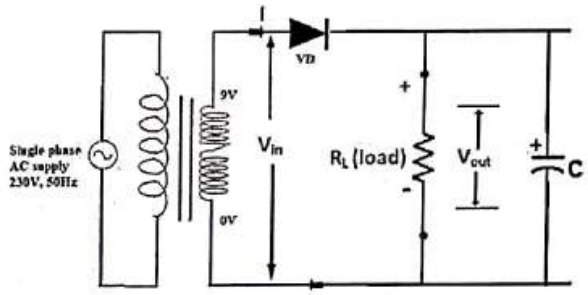
Half wave rectifier is one which converts the ac into pulsating dc during one half of the cycle. It has poor ripple factor, conversion efficiency and voltage regulation. Full wave rectifier is one which converts the ac into pulsating dc during both cycles. For this process two diodes and centre tapped transformer are required. It has better ripple factor, conversion efficiency and voltage regulation compared to the half wave rectifier.

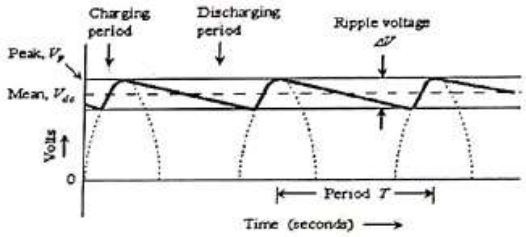
CIRCUIT DIAGRAM:

Half wave rectifier without filter:

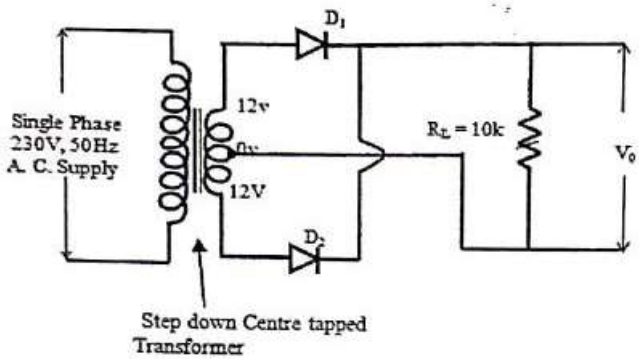


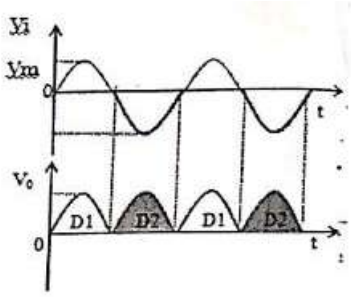
Half wave rectifier with filter



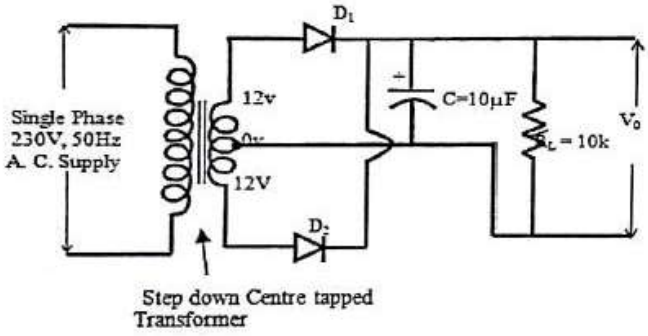


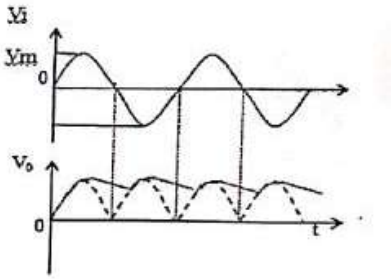
Full wave rectifier without filter





Full wave rectifier with capacitor –Filter





PROCEDURE:

1. Connect the components as shown in circuit diagram.
2. Note down the maximum value of output voltage (V_m) from the oscilloscope.
3. Calculate V_o(dc), V_o(rms), I_o(dc) & I_o(rms)
4. Find rectifier efficiency (n) and ripple factor (Y).
5. Connect the capacitor – filter across load resistor RL as shown in circuit diagram and calculate ripple factor (Y).

Tabular Column for HWR without filter:

R Load	Vac	Vdc	Ripple Factor	Efficiency %

Tabular Column for HWR with filter:

R Load	Vac	Vdc	Ripple Factor	Efficiency %

Tabular Column for FWR without filter:

R Load	Vac	Vdc	Ripple Factor	Efficiency %

Tabular Column for FWR with filter:

R Load	Vac	Vdc	Ripple Factor	Efficiency %

Experiment No. 3
Zener Diode as Voltage Regulator

AIM: To study the Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation.

COMPONENTS REQUIRED:

S.N	Particulars	Type	Range	Quantity
1.	Bread Board	---	---	01
2.	Zener Diodes	(IN4735A)	---	01
3.	Resistor	Carbon	1KΩ,3.3KΩ	01
4.	Digital Ammeter	---	0-200 mA	02
5.	Digital Voltmeter	---	0-20V	01
6.	Decade Resistance Box (DRB)	---	---	01
7.	Dual DC Regulated power supply	---	0-30V	01
8.	Connecting wires	Single strand	---	few

THEORY:

Zener diodes are a special kind of diode which permits current to flow in the forward direction. And also allow current to flow in the reverse direction when the voltage is above a certain value. This breakdown voltage is known as the Zener voltage.

In the forward bias direction, the zener diode behaves like an ordinary silicon diode. In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached. When this occurs there is a sharp increase in reverse current. Varying amount of reverse current can pass through the diode without damaging it. The breakdown voltage or zener voltage (V) across the diode remains relatively constant. The maximum reverse current is limited, however, by the wattage rating of the diode.

.

Zener Breakdown:

If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces compared to the width in normal doping. Applying a reverse bias causes a strong electric field get applied across the device. As the reverse bias is increased, the Electric field becomes strong enough to rupture covalent bonds and generate large number of charge carriers. Such sudden increase in the number of charge carriers due to rupture of covalent bonds under the influence of Strong electric field is termed as Zener breakdown.

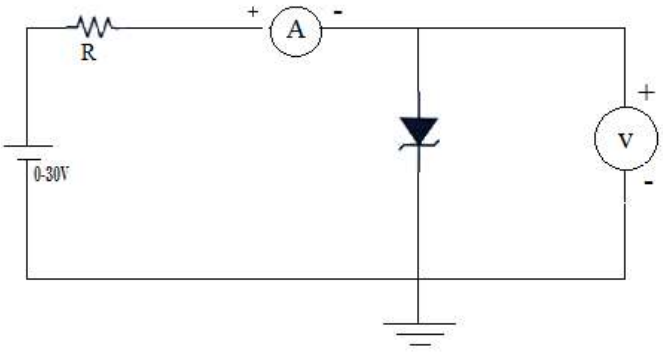
Zener Diode as Voltage Regulator:

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current.
Basically there are two types of regulation such as;

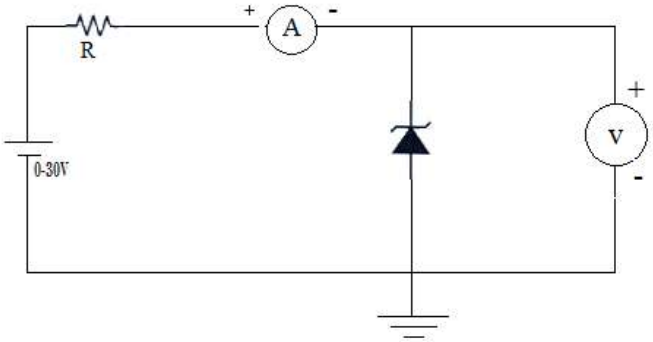
a. **Line Regulation:** This type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above minimum value.
b. **Load Regulation:** In this type of regulation, Input voltage is fixed and the load resistance is varying, Output voltage remains same, as long as the load resistance is maintained above a minimum value.

CIRCUIT DIAGRAM

Forward Characteristics



Reverse Characteristics



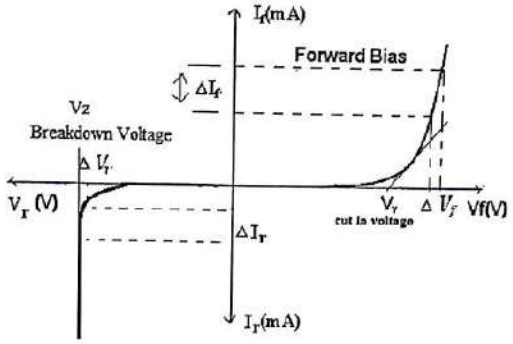


Fig: V-I Characteristics of Zener diode under forward and reverse bias conditions

PROCEDURE:

Forward Bias:

1. Connect the circuit as per the circuit diagram
2. Vary the power supply such that readings are taken in a step of 0.1V
3. Note down the corresponding Ammeter reading
4. Plot the graph of V_f V/s I_f

Reverse Bias:

1. Connect the circuit as per the circuit diagram
2. Vary the power supply such that readings are taken in a step of 0.5V
3. Note down the corresponding Ammeter reading
4. Plot the graph of V_r V/s I_r

TABULAR COLUMN:

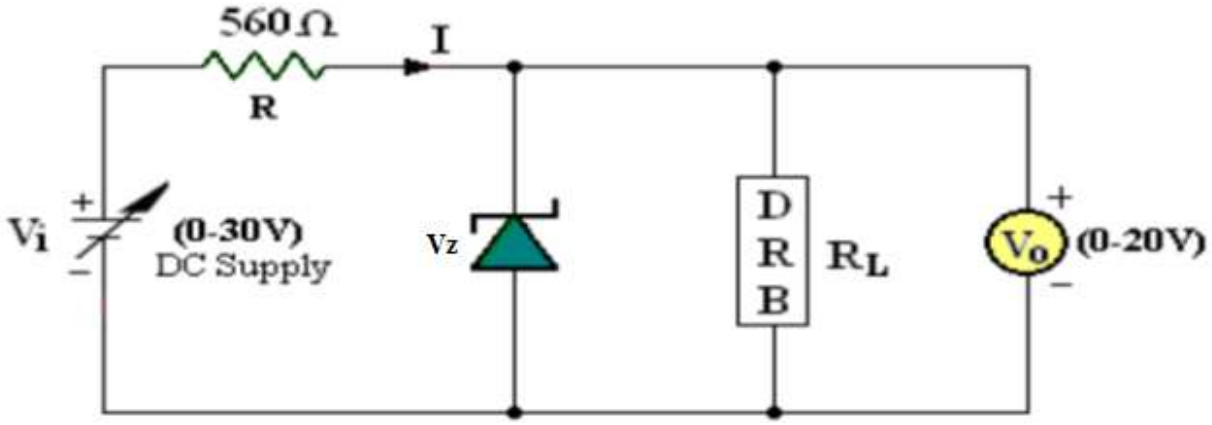
Forward Bias

Sl No	V_F	I_F

Reverse Bias

Sl No	V_R	I_R

Zener Diode as Voltage regulator



PROCEDURE:

Zener Diode as Line Regulator (for variations in supply voltage):

1. Rig up the Circuit as shown
2. For Voltage Regulation, Keep the load Resistance at 10KΩ, and change the input voltages. Take the readings of O/P Voltmeter (Vo=Vz).
3. Now fix the power supply voltage, V_i, at 10V.
4. Without connecting the load R_L, note down the No-Load Voltage (V_{NL}).

5. Now connect the load (R_L) using Decade Resistance Box (DRB) and vary the resistance in steps 1KΩ from IKΩ to 10KΩ / in steps of 10 KΩ from 10KΩ to 100 KΩ and note the corresponding Zener Current (I_Z), Load Current (I_L) and Output Voltage (V_O) for 10 readings and calculate the percentage regulation.
6. Plot the graph between R_L and V_O taking R_L on X-axis and V_O on Y-axis.

TABULAR COLUMN:

Line Regulation:

Load Resistance R_L = _____(KΩ)

Unregulated Power Supply V_S(V)	**Zener Current I_Z(mA)**	**Load Current I_L(mA)**	**Regulated Output Voltage V_O (V)**

Load Regulation:

Input Supply Voltage V_S = _____Volts
No-load DC Voltage, V_{NL} = _____Volts

Load Resistance R_L (KΩ)	**Zener Current I_Z(mA)**	**Load Current I_L (mA)**	**Regulated Output Voltage V_O(V)**	**% Voltage Regulation**

Calculations from Graph:

Static forward Resistance $R_{dc} = V_S/I_S\Omega$
Dynamic Forward Resistance $r_{ac} = \Delta V_S/\Delta I_S\Omega$
Static Reverse Resistance $R_{dc} = V_r/I_r\Omega$
Dynamic Reverse Resistance $r_{ac} = \Delta V_r/\Delta I_r\Omega$

For load regulations, % Voltage Regulation = ((VNL –VFL)/VFL) x 100 %

Experiment No: 4
CHARACTERISTICS OF LDR AND PHOTO DIODE AND TURN ON AN LED USING LDR

AIM: To determine the characteristics of LDR and Photo diode and tun on an LED using LDR

APPARATUS:

SL No	Components	Range	Quantity
1	Resistors	IKΩ, 10KΩ, 100KΩ, 10% tolerance, 1/2 watt rating	1
2	Photodiode	QSD 2030F	1
3	Phototransistor	BPW77NA	1
4	Regulated power supply	(0-30V), 2A Rating	1
5	Ammeter	(0-30)mA; (0-30) µA	1
6	Voltmeter	MC (0-10)V	1
7	LDR	---	1
8	Bread board	---	1
9	Connecting wires	---	Few

`

THEORY:

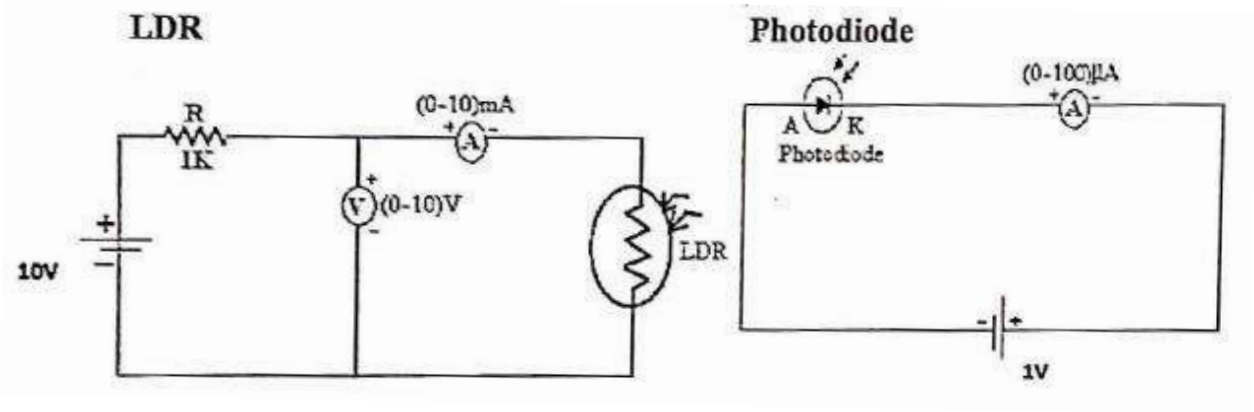
LDR

A photoresistor or light dependent resistor or cadmium sulfide (CdS) cell is a resistor whose resistance decreases with increasing incident light intensity. It can also be referred to as a photoconductor. A photoresistor is made of a high resistance semiconductor. If light falling on the device is of high frequency, photons absorbed by the semiconductor gives enough energy to for electrons to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance

Photodiode

A silicon photodiode is a solid state light detector that consists of a shallow diffused P-N junction with connections provided to the outside world. When the top surface is illuminated, photons of light penetrate into the silicon to a depth determined by the photon energy and are absorbed by the silicon generating electron-hole pairs. The electron-hole pairs are free to diffuse (or wander) throughout the bulk of the photodiode until they recombine. The average time before recombination is the minority carrier lifetime. At the P-N Junction is a region of strong electric field called the depletion region. It is formed by the voltage potential that exists at the P-N junction. Those light generated carriers that wander into contact with this field are swept across the junction. If an external connection is made to both sides of the junction a photo induced current will flow as long as light falls upon the photodiode. In addition to the photocurrent, a voltage is produced across the diode. In effect, the photodiode functions exactly like a solar cell by generating a current and voltage when exposed to light.

CIRCUIT DIAGRAM:



TABULAR COLUMN

LDR

Distance(cm)	Voltage(V)	Current(mA)	Resistance(KΩ)=V/I

Photodiode

SL NO	Without Light		With Light	
	Reverse voltage V_R in V	Reverse current IR in mA	Reverse voltage V_R in V	Reverse current I_R in mA

PROCEDURE:

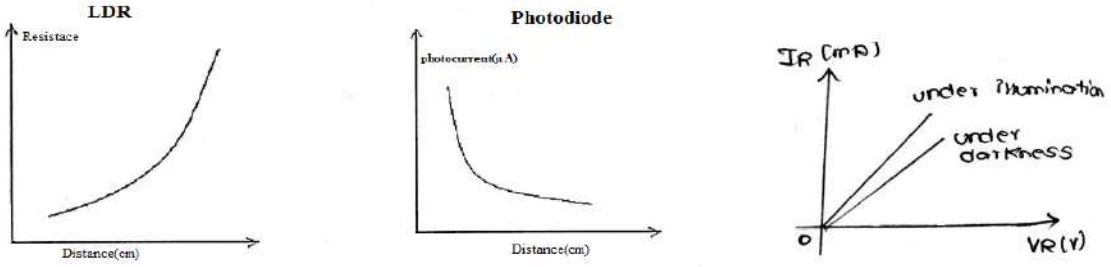
LDR:

1. Connect circuit as shown in figure
2. Keep light source at a distance and switch it ON, so that it falls on the LDR
3. Note down current and voltage in ammeter and voltmeter.
4. Vary the distance of the light source and note V&I
5. Sketch graph between R as calculated from observed V and I and distance of light source

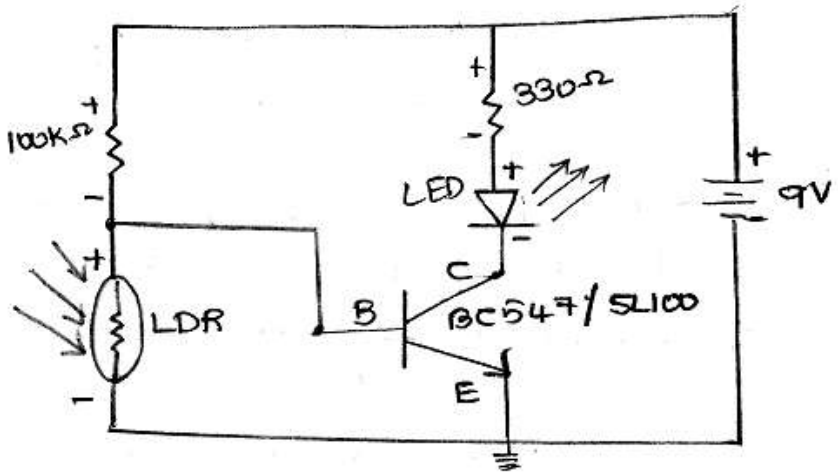
Photodiode:

1. Connect circuit as shown in figure
2. Maintain a known distance between the bulb and photodiode say 5cm
3. Set the bulb voltage, vary the voltage of the diode in steps of 1V and note the diode current I_R.
4. Repeat above procedure for V_L=4V, 6V, etc.
5. Plot the graph: V_D V_S I_R for constant V_L

Model Graph:



Circuit to switch ON /OFF an LED using LDR



Experiment No. 5
STATIC CHARACTERISTICS OF SCR

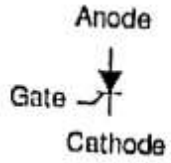
AIM: To conduct and plot V-I static characteristics of SCR and determine Latching current and Holding current.

APPARATUS:

SLNO	Components	Range	Quantity
1	DC Power Supply	0-30V	2
2	Resistor	100Ω	1
3	SCR	100KΩ	1
4	DC voltmeter	(0-20) V	1
5	DC ammeter	(0-200) mA (0-200)μA	1
6	Connecting wires		Few

THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J1, J2, J3 the Jl and J3 operate in forward direction and J2 operates in reverse direction and three terminals called anode A, cathode K , and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J2 no current flows through R2 and hence SCR is at cut off. When anode voltage is increased J2 tends to breakdown.

When the gate positive, with respect to cathode J3 junction is forward biased and J2 is reverse biased. Electrons from N-type material move across Junction J3 towards gate while holes from P-type material moves across junction J3 towards cathode. So gate current starts flowing, anode current increases.

When gate is open, the break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current when gate being open, when break over occurs.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Set both voltage sources to zero volts.

To find minimum gate current,

3. Set V_{AK} from 10 to15 V. Slowly vary V_{AK} in steps of 1V. Note down the corresponding I_G and I_{AK} values.
4. At some point, I_{AK} is suddenly increased and V_{AK} decreases.
5. Note down the minimum gate current required to turn on SCR.
6. Set both voltage sources to zero volts.

V I Characteristics

7. Set the minimum gate current in terms of mA
8. Slowly vary $V_{AK,}$ note down corresponding values of $I_{AK,}$
9. Draw the graph V_{AK}V/S I_{AK}

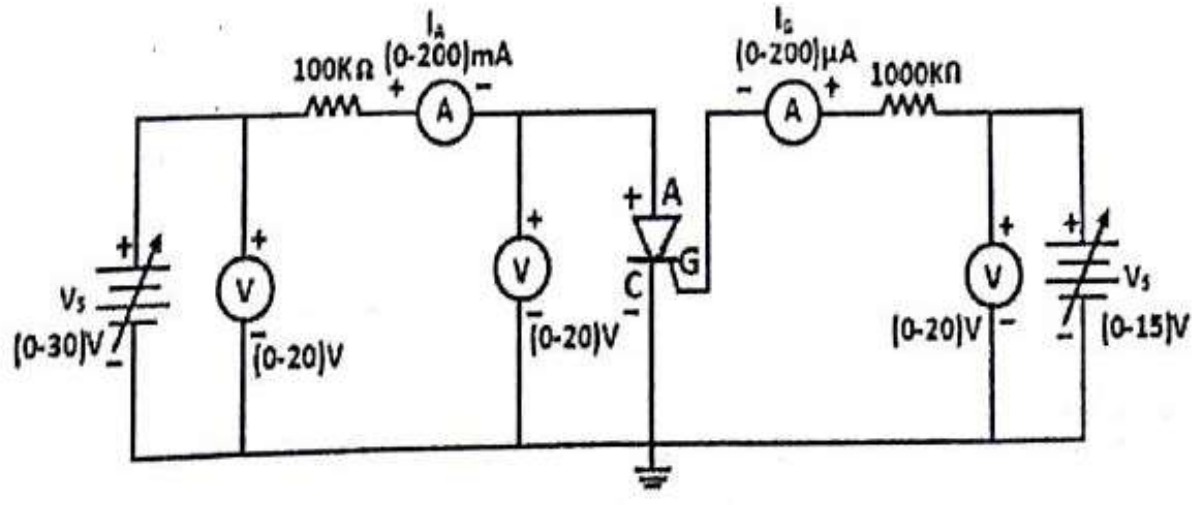
To find Latching current

10. Set V_{AK} and V_{GK} in minimal position
11. Switch on power supply vary V_{AK} and set I_G
12. Slowly vary V_{AK} , note down the corresponding values of I_{AK} and simultaneously remove the gate pulse and check the state of SCR(ON/OFF)
13. If the SCR is ON even if gate pulse is removed, then the corresponding current is called latching current.

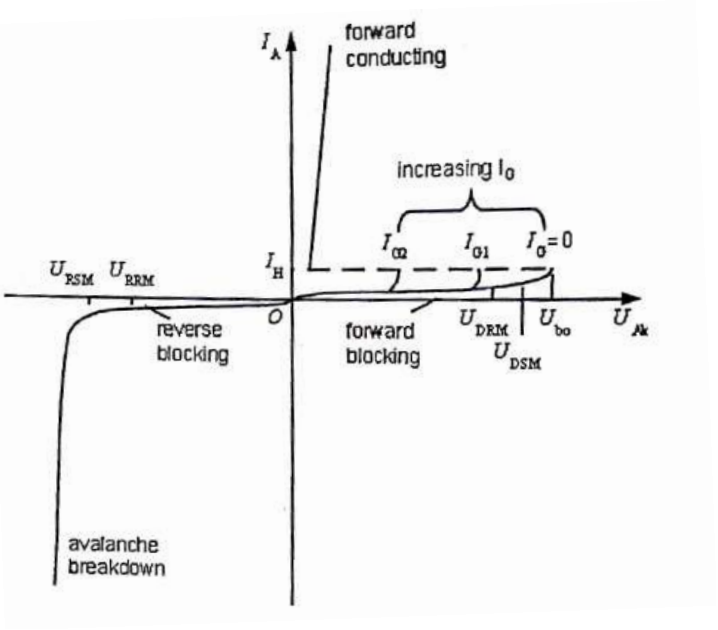
To find holding current

14. Turn on SCR by normal method.
15. Decrease V_{AK} gradually
16. Note down Anode current at which SCR turns OFF. Corresponding Anode current is the holding

CIRCUIT DIAGRAM:



EXPECTED GRAPH:



TABULAR COLUMN:

SL NO	Gate current= _____µA		Gate current= _____µA	
	Anode to cathode voltage	Anode current	Anode to cathode voltage	Anode current

RESULT:

Static characteristics of SCR is analysed
Latching current is ……
Holding current is ……

Experiment No. 6
SCR controlled HWR and FWR using RC Triggering circuit

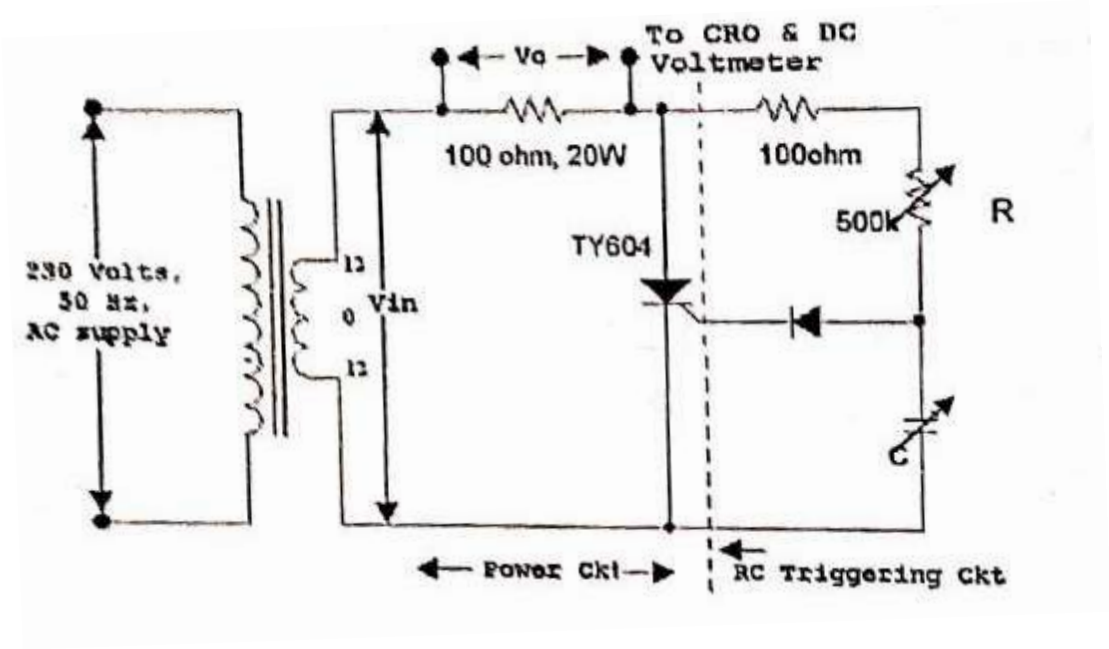
AIM: To study the performance and waveforms of HWR & FWR by using RC triggering circuit

APPARATUS:

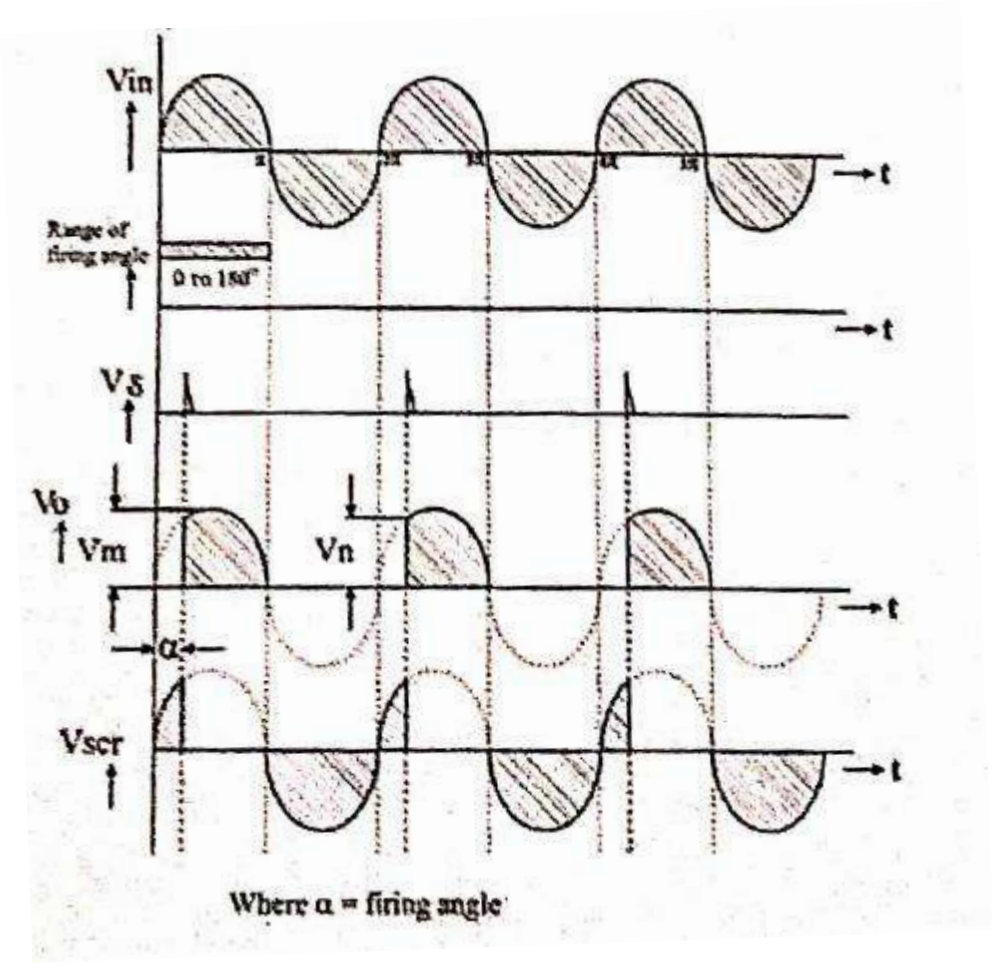
SL No	Components	Range	Quality
1	DC Power Supply	0-30V	2
2	Resistor	100Ω	1
3	Transformer	230V, 50Hz	1
4	SCR Diode	TY604 BY127	1
5	DC voltmeter	(0-20)V	1
6	DC ammeter	(0-200)mA (0-200)µA	1
7	Connecting wires		

CIRCUIT DIAGRAM:

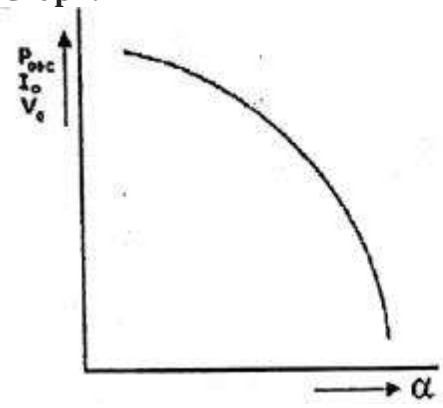
Half wave rectifier:

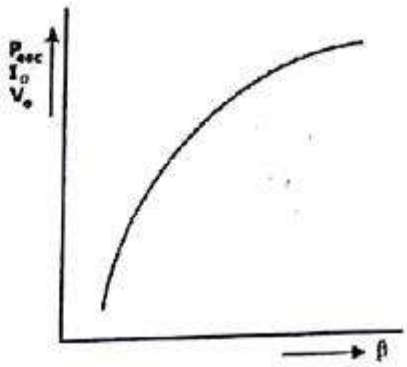


Waveforms:

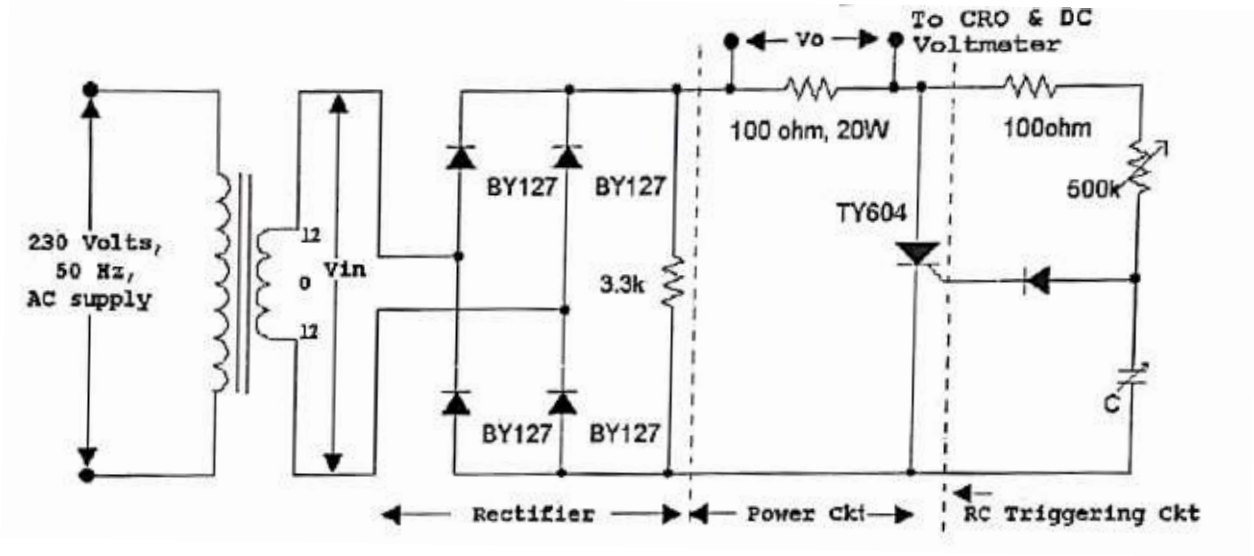


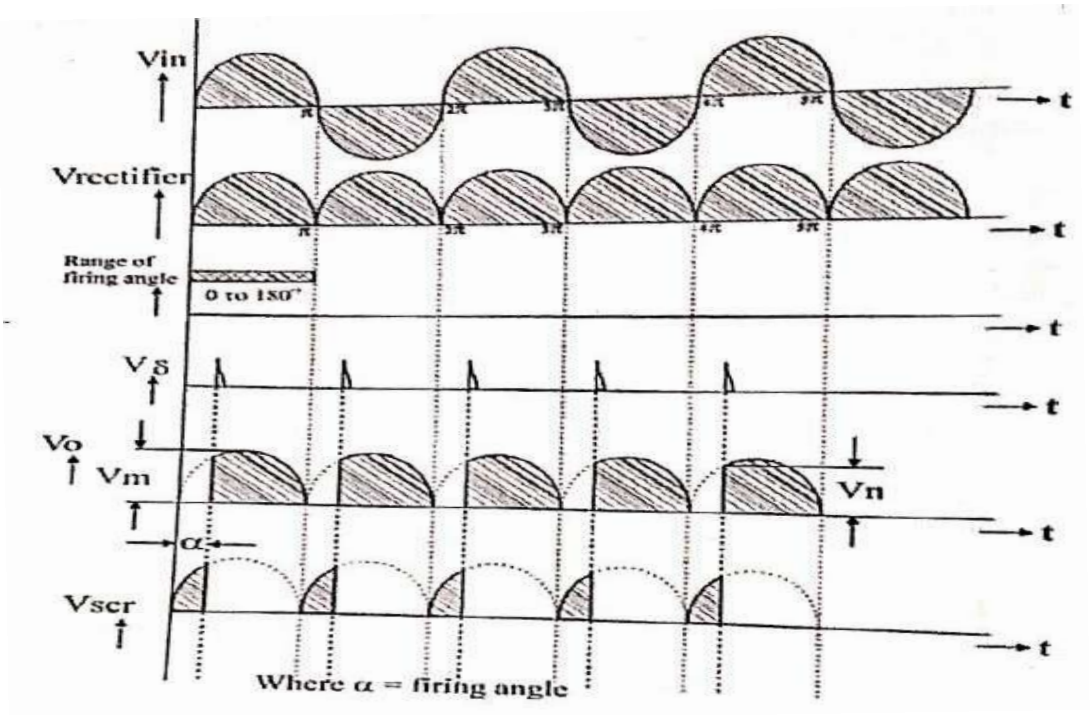
Graph:





Full wave rectifier:





PROCEDURE:

Half wave rectifier:

1. Connections are made as shown in the circuit diagram.
2. By varying a resistance R gradually step by step, note down the corresponding values of V_n & V_m from CRO and $V_{o\,dc}$ from the DC voltmeter. The readings are tabulated in the tabular column.
3. If the firing angle ranges from 0 to 90°, then the firing angle α is calculated by using a formula $\alpha = \sin^{-1}(V_n/V_m)$ in degrees.
4. The conduction angle β is calculated by using a formula, $\beta = 180 - \alpha$.
5. The current and power is calculated by
   $I_{o\,dc} = (V_{o\,dc}/R)$ in A & $P_{o\,dc} = V^2_{odc}/R$ in watts respectively.
6. A graph of Vo v/s α, Vo v/s β, Io v/s α, lo v/s β, $P_{o\,dc}$ v/s α, $P_{o\,dc}$ v/s β to be plotted.
7. Compare practical output voltage with theoretical output voltage,
   $V_{oth} = V_m(1+\cos\alpha)/2\pi$ volts where $V_m = \sqrt{2}V_{rms}$

Full wave rectifier:

1. Repeat the above said procedure for full wave rectifier.
   $V_{oth} = V_m(1+\cos\alpha)/\pi$ volts where $V_m = \sqrt{2}V_{rms}$

TABULAR COLUMN:

Half wave rectifier

SL No	V_n	V_m	α < 90 degree	α> 90 degree	V_{odc}	V_{oth}
			$\alpha=\sin^{-1}(V_n/V_m)$	$\alpha=180 - \sin^{-1}(V_n/V_m)$		

Full wave rectifier

SL No	V_n	V_m	α < 90 degree	α> 90 degree	V_{odc}	V_{oth}
			$\alpha=\sin^{-1}(V_n/V_m)$	$\alpha=180 - \sin^{-1}(V_n/V_m)$		

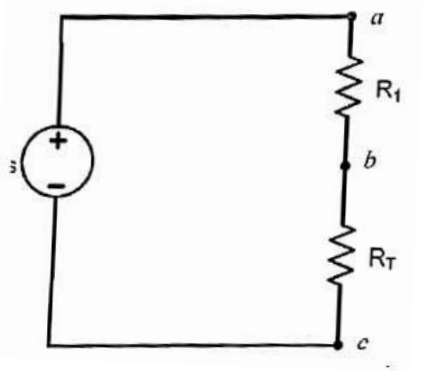
Experiment No. 7
TEMPRATURE SENSOR BRIDGE CIRCUITS

AIM: To implement Wheatstone bridge circuits for temperature measurements using thermistors

THEORY:

A. Voltage Dividers

Using resistors R_1 and R_T, the voltage can be split depending on the ratio between the two resistors.



$$I_{ab} = I_{bc}, \quad V_s = V_{ab} + V_{bc} \rightarrow \frac{V_{ab}}{R_1} = \frac{V_{bc}}{R_T}$$

$$V_s = \frac{R_1}{R_T} V_{bc} + V_{bc}$$

$$V_{bc} = \frac{R_T}{R_1 + R_T} V_s$$

Application: If R_T is the resistance of a "resistance sensor", e.g. an RTD (resistance temperature detector), a thermistor or a strain gauge, one can measure changes in R_T by measuring V_{bc} (with V_S and R_1 fixed).

B. Wheatstone Bridge

Main idea: By adding another (comparator) voltage divider in parallel to that shown in Figure, one could use differential voltage measurements around zero for improved sensitivity in sensor applications, while reducing current flow through component R_T.

(Note that high electrical currents increase heat in resistors. These effects introduce measurement errors since they are unrelated to the variables being measured).

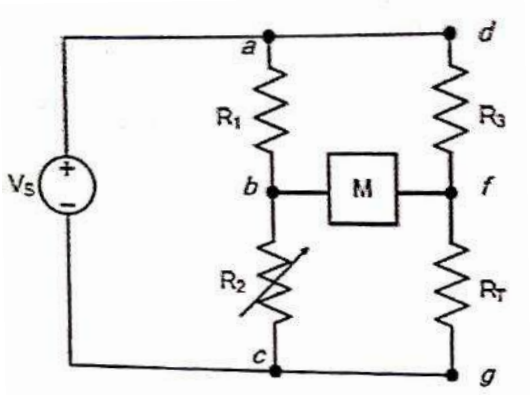


Figure 2: Wheatstone bridge. (M is the voltmeter)

Assuming that very little current flows through the voltmeter, i.e. setting Ifb=0,

$$\begin{aligned} I_{ab} &= I_{bc} \\ I_{df} &= I_{fg} \end{aligned} \rightarrow \begin{aligned} \frac{V_{ab}}{R_1} &= \frac{V_{bc}}{R_2} \\ \frac{V_{df}}{R_3} &= \frac{V_{fg}}{R_T} \end{aligned} \rightarrow \begin{aligned} V_{ab} &= V_{bc}\frac{R_1}{R_2} \\ V_{df} &= V_{fg}\frac{R_3}{R_T} \end{aligned} \qquad (2)$$

Summing voltages around each loop.

$$\begin{aligned} V_s &= V_{ab} \div V_{bc} \\ V_{ab} &= V_{df} \div V_{fb} \\ V_{bc} \div V_{fb} &= V_{fg} \end{aligned} \rightarrow \quad V_s = V_{ab} + V_{bc} = V_{df} + V_{fg} \qquad (3)$$

Substituting (2) into (3),

$$V_s = V_{bc}\left(1+\frac{R_1}{R_2}\right) = V_{fg}\left(1+\frac{R_3}{R_T}\right) \qquad (4)$$

Applying (4) to the loop containing V_{bc}, V_{fb} and V_{fg},

$$\begin{aligned} V_{fb} &= V_{fg} - V_{bc} \\ &= V_s\left(\frac{1}{1+\frac{R_3}{R_T}} - \frac{1}{1+\frac{R_1}{R_2}}\right) \qquad (5) \\ &= V_s\left(\frac{R_T}{R_T+R_3} - \frac{R_2}{R_2+R_1}\right) \end{aligned}$$

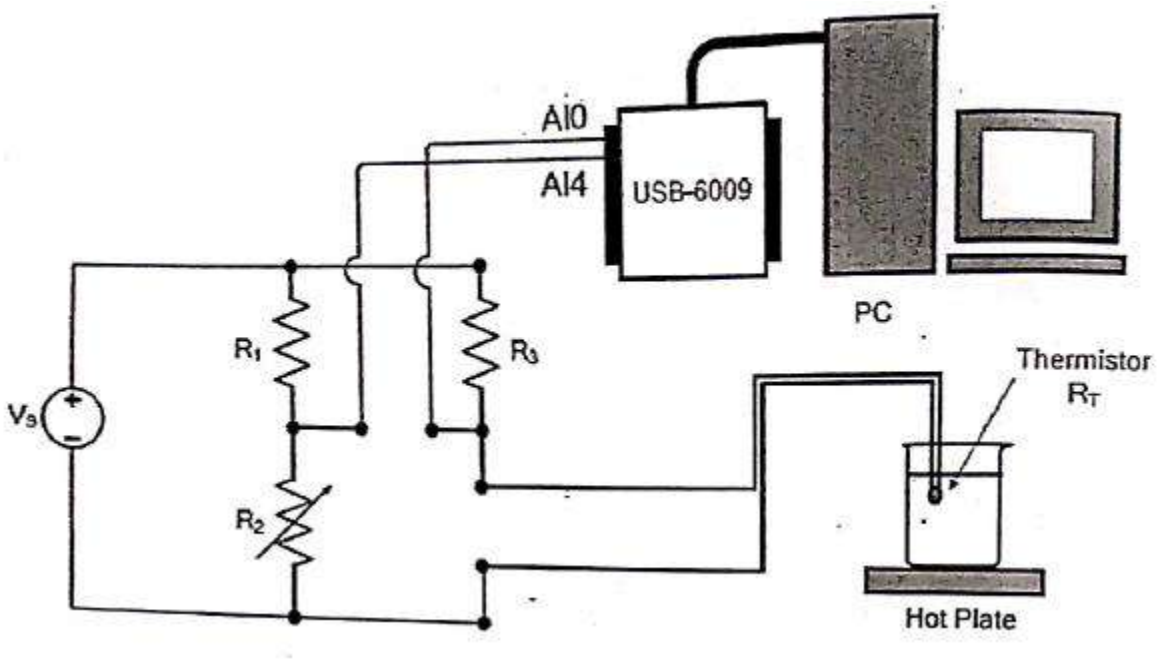
The bridge is "balanced" when V_{fb}=0, i.e. voltage reading in meter M is zero. This occurs when

$$\frac{R_3}{R_T} = \frac{R_1}{R_2}.$$

Since R_2 is a variable resistor, the meter can be zeroed around the nominal value of the variable being sensed. For instance, if the component is an RTD, then the bridge is balanced around a nominal operating temperature T_0. Voltage readings of V_{fb} can then monitor temperature changes from T_0.

R_1	4.7 KΩ
R_2	10 KΩ potentiometer
R_3	4.7 KΩ
V_S	6 V power supply
Thermistor	~2.80 KΩ @ 25°C

CIRCUIT DIAGRAM:



PROCEDURE:

1. Prepare the setup shown in Figure and the Thermistor VI as well.
2. Note down the voltage readings for different temperature using multi meter.

Temperature (°C)	Voltage (volts)
30	
35	
40	
45	
50	
55	
60	
65	

Experiment No. 8
MEASUREMENT OF RESISTANCE USING WHEATSTONE BRIDGE AND KELVIN'S BRIDGE

AIM: To measure the given unknown resistance using Wheatstone bridge Kelvin's bridge.

APPARATUS:

SL NO	Components	Range	Quality
1	DC Power Supply	---	1
2	Few Resistors	100Ω, 1 K Ω, 10 K Ω	1
3	Galvanometer	---	1
4	Multimeter	---	1

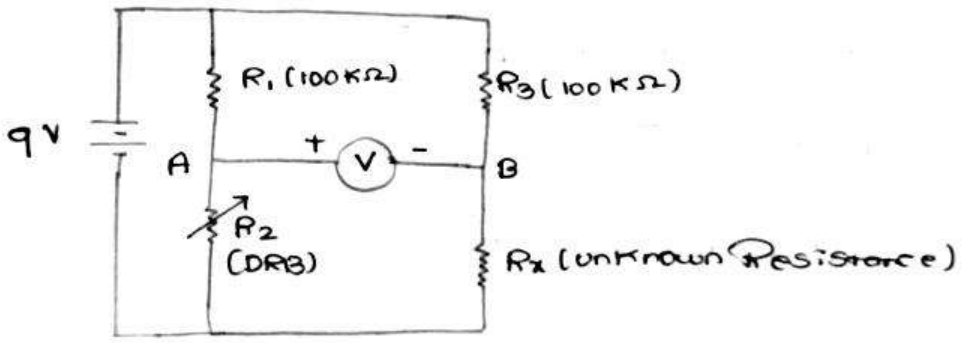
THEORY:

A wheat stone bridge is an electrical circuit used to measure an unkown resistance by balancing two legs of bridge circuit, one leg of which include the unknown components. Practically the variable resistance is adjusted till the value of galvanometer becomes Zero. At this point , bridge is said to be balanced.

At balanced condition, $R_1/R_2=R_3/Rx$

$Rx= R_2 R_3/ R_1$

CIRCUIT DIAGRAM:



$$\text{Error} = \frac{\text{Actual value} - \text{obtained value}}{\text{Actual value}} \times 100$$

PROCEDURE:

1. Use 9V battery and take $R_1 = R_3$
2. Connect the Circuit as Shown
3. The value of DRB is adjusted till the value of voltage displayed on the meter was closed to 0V
4. At some point, the value of decade resistance box is matched to the value of unknown resistance with 5to 10% of tolerance.

TABULAR COLUMN:

SL NO	R_1 **(Ω)**	R_2 **(Ω)**	R_3 **(Ω)**	Rx **(Ω)**

KELVIN BRIDGE:

CIRCUIT DIAGRAM:

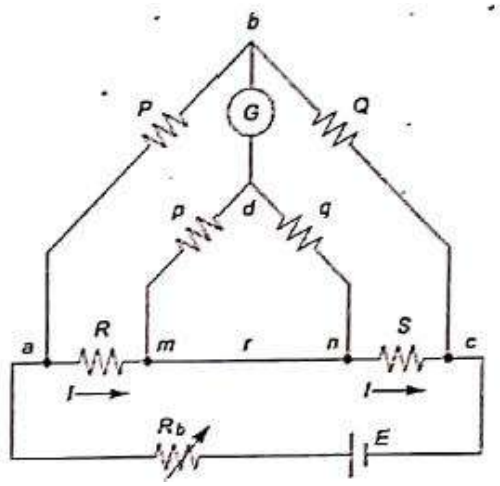


Figure: Simplified kelvin Bridge Circuit

A Kelvin Bridge is a measuring instrument used to measure unknown electrical resistors below 1Ω. It is specifically designed to measure resistors that are constructed as four terminal resistors.

The operation of the Kelvin Bridge is very similar to the Wheatstone bridge except that it is complicated by the presence of two additional resistors; Resistors P and Q are connected to the outside potential terminals of the four terminal known or standard resistors S and the unknown resistor R. The resistors S, R, P and Q are essentially a Wheatstone bridge. Is this arrangement, the parasitic resistance of the upper part of S and the lower part of R is outside of the potential measuring part of the bridge and therefore re not included in the measurement. However, the link between S and is included in the potential measurement part of the circuit and therefore can affect the accuracy of the result. To overcome this, a second pair of resistors 'p' and 'q' form a second pair of arms of the bridge (hence 'double bridge) and are connected to the inner potential terminals of S and R The detector D is connected between the junction of P and Q and the junction of p and q

The balance equation of this bridge is given by the equation

$$R= (P/Q)\ S+qr/(p+q+r)\ [P/Q-(p/q)]$$

As per the design P/Q= p/q, the value of unknown resistance is,

$$R= (P/Q\ )S$$

Above equation is the usual working equation for the Kelvin double bridge. It indicates that resistance of connecting lead r has no effect on the measurement provided that the two sets of ratio arms have equal ratios. The above equation is useful however 85 South error that is introduced in case the ratios are not exactly equal It is indicated that it is desirable to keep as small as possible in order to minimize the errors in case there is a difference between ratios P / Q and p/q. In a typical Kelvin bridge, the range of resistance calculated is 0.1Ω to 1.0 Ω.

PROCEDURE:

1. Connections are made as per the connection diagram
2. Connect the unknown resistance at R terminals.
3. Switch ON the unit.
4. Select the range selection switch at the point where the meter reads least possible value of voltage.
5. Vary the potentiometer (S) to obtain null balance
6. Switch OFF the unit and find the resistance using multimeter at S.
7. Tabulate the readings and find the value of unknown resistance using the above formula
8. Repeat the above for different values of unknown resistors.

TABULAR COLUMN:

SL NO	**P(Ω)**	**Q(Ω)**	**R(Ω)**	**S(Ω)**

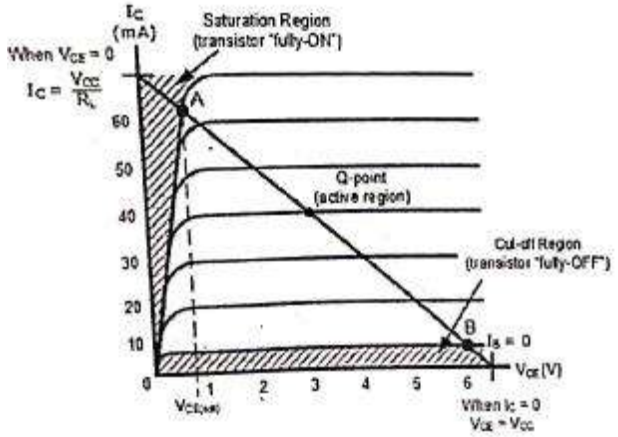
Experiment No.:9
Characteristics of BJT

AIM: To determine the Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.

THEORY: A Bipolar Junction Transistor (BJT) has three terminals connected to three doped semiconductor regions. In an NPN transistor, thin and lightly doped P-type base is sandwiched between a heavily doped N-type emitter and another N-type collector, while in a PNP transistor, a thin and lightly doped N-type base a sandwiched between a heavily doped P-type emitter and another P-type collector.
The output characteristics show the relationship between the collector current (IC) and the collector-emitter voltage (VCE) with the varying of base current (IB)

The collector current (IC) is mostly affected by the collector voltage (VCE) at 1.0V level but this IC value is not highly affected above this value. Already we know that the emitter current is the sum of base and collector current. In. IE = IC+ IB. The current flowing through the resistive load (RL) give to the collector current of the transistor The equation for the collector current is given by,

$$I_C = (V_{CC}-V_{CE})\, R_L$$

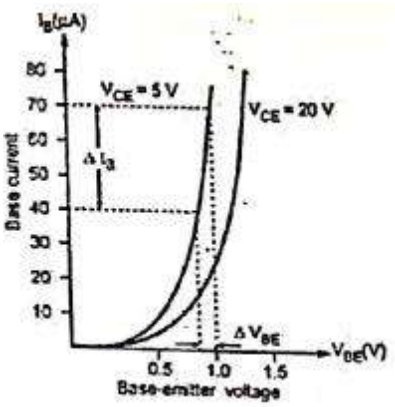


The straight line indicates the 'Dynamic load line' which is connecting the points (where V_{CE}=0) and B (where I_C= 0). The region along this load line represents the 'active region' of the transistor.

The common emitter configuration characteristics curves are used to calculate the collector current when the collector voltage and base current is given. The load line (red line) is used to determine the Q- point in the graph. The slope of the load line is equal to the reciprocal of the load resistance.
i.e -I/R_L

$$R_{out} = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B=constant}$$

Input Characteristics



It is the curve between input current I_B and input voltage V_{BE} at constant collector-emitter voltage, V_{CE} Fig shows the input characteristics of a typical transistor in common-emitter configuration.

This ratio is referred to as common-emitter current gain and is always greater than 1.

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}=constant}$$

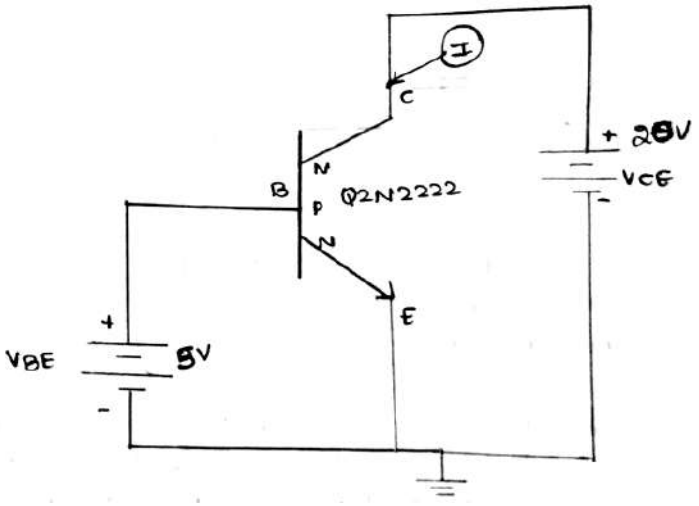
The current gain in common base configuration α is

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=constant}$$

related to β as $\beta = \alpha/(1-\alpha)$ and $\alpha = \beta/(1+\beta)$

The value of α is always less than unity.

CIRCUIT DIAGRAM:



PROCEDURE :

Input Characteristics

1. Construct the circuit as shown in Figure.
2. From the main menu, select Simulate → Analysis → DC Sweep
3. Set the Analysis Parameters tab as follows:
   - Set The Source to be V_{BE}
   - Start value: OV.
   - Stop value: 5V.
   - Increment: 0.1V
4. Set the nested source to be V_{CE}
   - Start value: 0V.
   - Stop value: 20V.
   - Increment: 2V

5. Click the Output tab, select V(V_1+:A)
6. Click Simulate, a grapher window will pop up after simulation is complete, showing the input Characteristics of BJT.

Output Characteristics

1. Construct the circuit as shown in Figure.
2. From the main menu, select Simulate >Analysis >DC Sweep
3. Set the Analysis Parameters tab as follows:
   Set the Source to be VCE
   Start value: 0 V
   Stop value: 20V.
   Increment: 1V
   Set the nested source to be VBE
   Start value: 0V.
   Stop value: 5V
   Increment: 0.1V

5.Click Simulate, a graph window will pop up after simulation is complete, showing the output Characteristics of BJT.

Result:

The input and output characteristics of BJT is simulated using PSPICE

Experiment 10
Transfer and drain characteristics of a JFET and MOSFET

AIM: To plot the characteristics of JFET and MOSFET and to calculate its parameter.

THEORY:

The JRET is a unipolar device because its operation depends only on one type of carriers. JFET has high input impedance unlike BJT.

The JFET are two types N-channel JFET and P-channel JFET, An N-channel JFET is an N-type silicon bar with a P-type semiconductor embedded on both sides of the bar, The P-type semiconductor forms the gate and the ends of the N-type bar are source and drain. The P-type region are internally shorted. The gate of an N-channel JFET is connected to positive potential with respect to the source.

Drain dynamic resistance r_d

The drain dynamic resistance is defined as the ratio of change in drain to source voltage to the change in drain current, when gate to source voltage remain constant.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{constant}}$$

Mutual Conductance

The mutual conductance is defined as the ratio of change in drain current to the change in gate to source voltage, when drain to source voltage remains constant

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ \text{constant}}$$

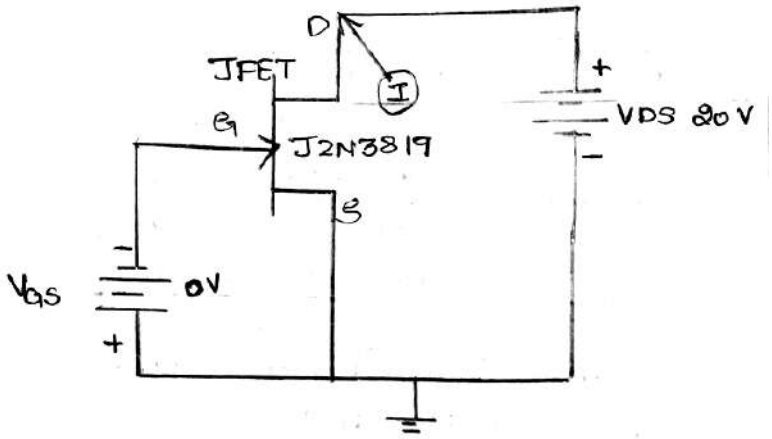
Amplification factor

It is defined as the ratio of change in drain to source voltage to the change in gate to source voltage when drain current remains constant.

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D\ \text{constant}}$$

Where μ ,g_m and r_d are related to each other as $\mu = g_m x\ r_d$

SIMULATION CIRCUIT DIAGRAM



MOSFET

In a MOSFET, current flows from the drain terminal to the source terminal through semiconductor channel. The resistance of the channel, and therefore its ability to conduct current, is controlled by a voltage applied to a third terminal denoted as the gate. MOSFET can be either an n-channel type or a p-channel type. In an n-channel MOSFET a positive voltage is applied to the drain terminal for operation while in a p-channel MOSFET a negative voltage is applied to the drain terminal for operation. A D-channel and p-channel type MOSFET may be one of two modes; enhancement mode or depletion mode. The enhancement mode MOSFET is normally (in cut-off and conducting no current) when no voltage is applied to the gate and is "on" (in saturation and conduction current) when a voltage greater than the gate-to source threshold is applied to the gate. The depletion mode MOSFET normally "on" (in saturation and conduction current) when no voltage is applied to the gate and is "off" (in cut-off and not conducting current) when a voltage more negative than the gate-to-source threshold is applied to the gate

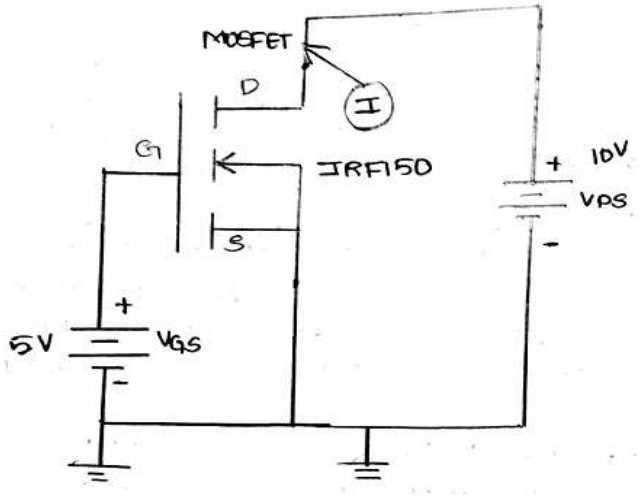
Transfer Characteristics:

In most MOSFET applications, an input signal is the gate voltage VG and the output is the drain current ID. The ability of MOSFET to amplify the signal is given by the output/input ratio: the trans conductance, gm= dID/dVGS with VDS constant

Drain Characteristics:

MOSFET operates in three operation mode, Cut-off when VGS<Vt, Linear mode when VGS > Vth and VDS< (VGS-Vth) and Saturation when VGS >Vth and VDS ≥ (VGS- Vth). Pinch off occurs when VDS=VSat= VGS-Vth. The drain resistance, Rd=dVDS/dID with VGS-constant

SIMULATION CIRCUIT DIAGRAM



PROCEDURE:

Transfer Characteristics

1. Construct the circuit as shown in Figure.
2. From the main menu, select Simulate →Analysis →DC Sweep
3. Set the Analysis Parameters tab as follows:
   - Set the Source to be VGS (put all -ve value for JFET and +ve for MOSFET)
   - Start value: 0V.
   - Stop value: 5V.
   - Increment: 1V
4. Set the nested Source to be VDS
   - Start value: 0V.
   - Stop value: 20V.
   - Increment: 5V
5. Click Simulate, a graph window will pop up after simulation is complete, shows the transfer Characteristics of JFET/MOSFET.

Drain Characteristics

1. Construct the circuit as shown in Figure
2. From the main menu, select Simulate →Analysis →DC Sweep
3. Set the Analysis Parameters tab as follows
   - Set the Source to be VDS
   - Stan value: 0V
   - Stop value: 20V.
   - Increment: 5V
4. Set the nested Source to be VGS
   - Start value: 0V.
   - Stop value: 5V.
   - Increment: 1V
5. Click Simulate, a graph window will pop up after simulation is complete, showing the drain Characteristics of JFET/MOSFET

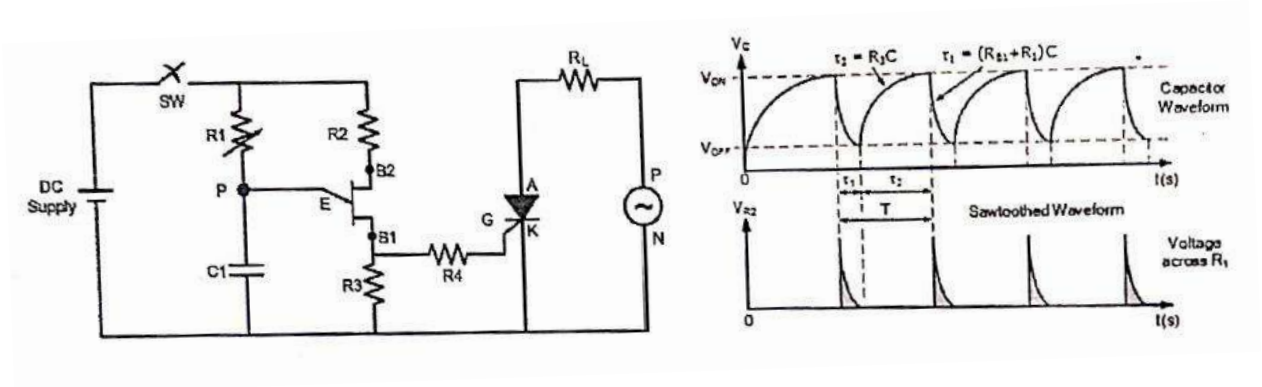
Result : Tansfer and drain characteristics of JFET and MOSFET are simulated.

Experiment 11
UJT triggering circuit for Controlled Rectifiers

AIM: Design and setup UJT triggering circuit for a single-phase half wave Controlled Rectifiers.

THEORY:

A un-junction transistor (UJT) is an electronic semiconductor device that has only one junction.The UJT has three terminals: an emitter (E) and two bases (Bl and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.



When the voltage across the capacitor reaches the UJT triggering voltage, the UJT turns ON. At this instant, the capacitor discharges through emitter (E), base (BI) and primary of pulse transformer. A pulse is produced at the primary, as well as at the secondary's of the transformer.

When the capacitor discharges to a voltage called valley voltage the UJT turns-off and capacitor charges again and the whole process repeats itself. The charging of the capacitor can be varied by varying the value of resistance R and therefore the firing angle can be controlled from 0 to 180 Degrees.

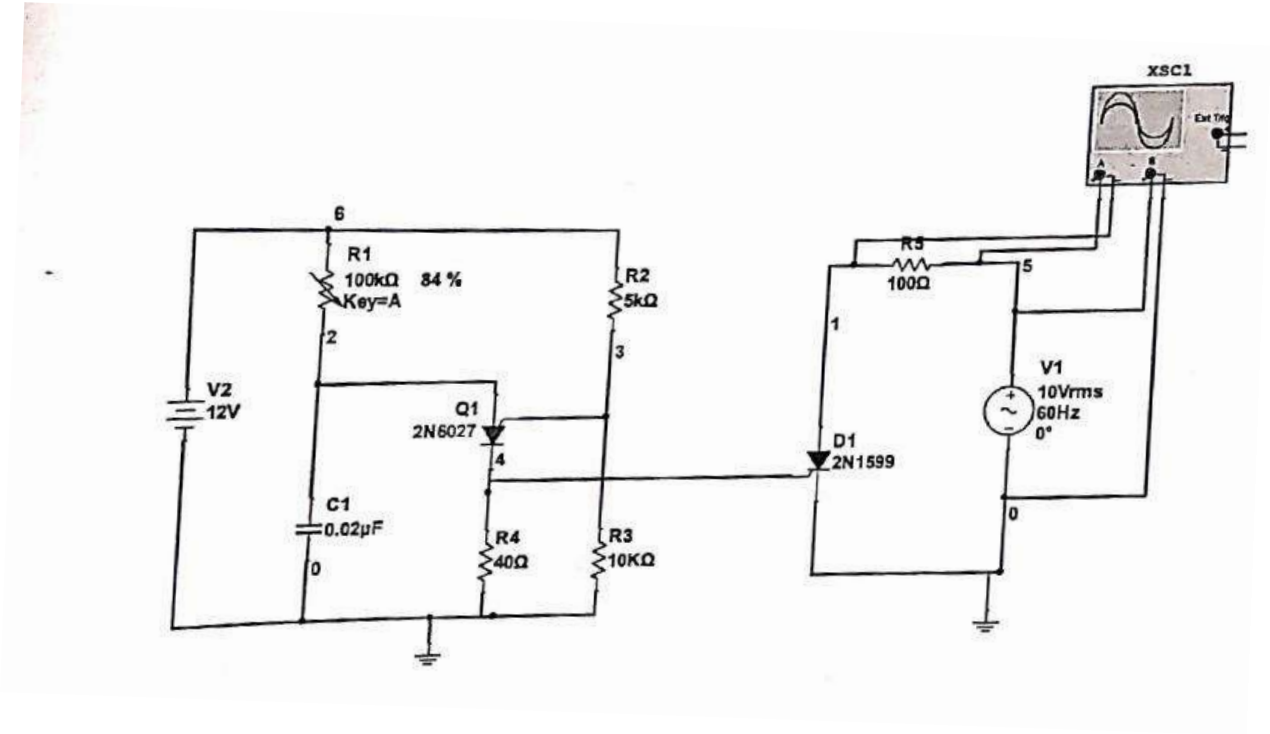
Then we can see that the un-junction oscillator continually switches "ON" and "OFF" without any feedback. The frequency of operation of the oscillator is directly affected by the value of the charging resistance R1, in series with the capacitor Cl and the value of ɳ. The output pulse shape generated from the Basel (BI) terminal is that of a saw-tooth waveform and to regulate the time period, you only have to change the Ω value of resistance, R1 since it sets the RC time constant for charging the capacitor.

The time period, T of the saw-toothed waveform will be given as the charging time plus the discharging time of the capacitor. As the discharge time t_1, it is generally very short in comparison to the larger RC charging time, t_2 the time period of oscillation is more or less equivalent to $T \approx t_2$. The frequency of oscillation is therefore given by f=1/T.

PROCEDURE:

1. Construct the circuit diagram as shown in figure

2. Run the simulation and observe the waveform at different firing angle by varying R1 resistor.



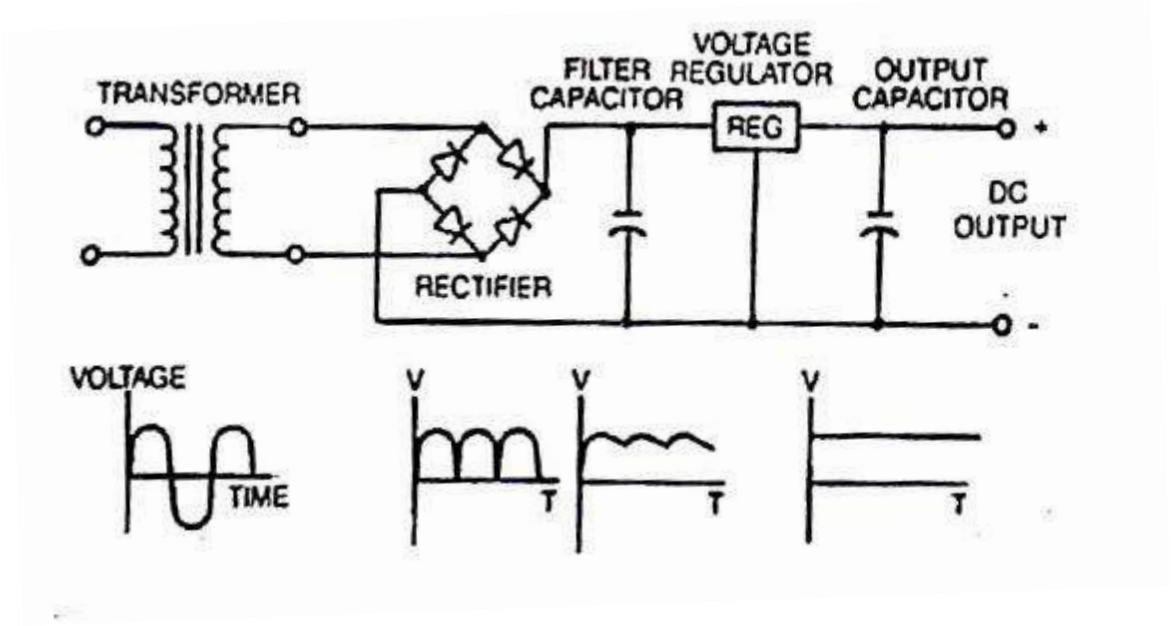
Experiment 12
Regulated power supply

AIM: Design and simulation of Regulated power supply.

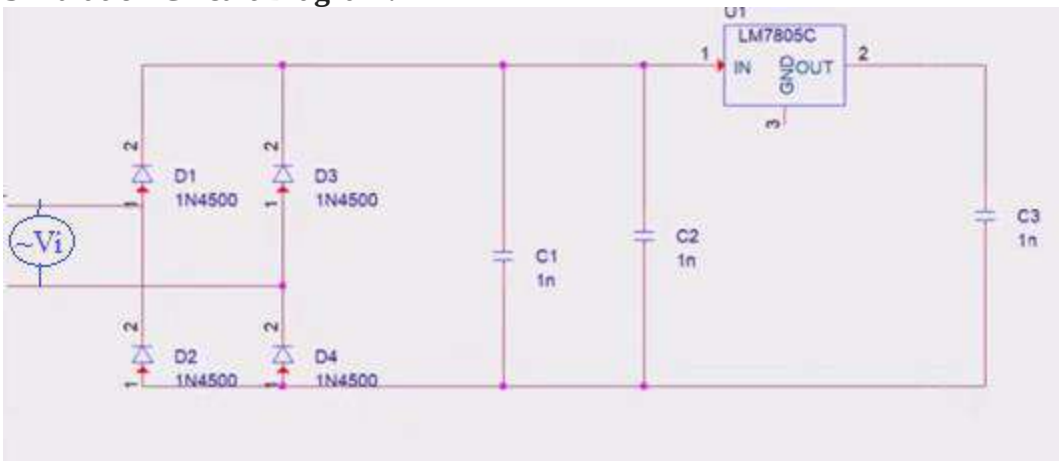
THEORY:

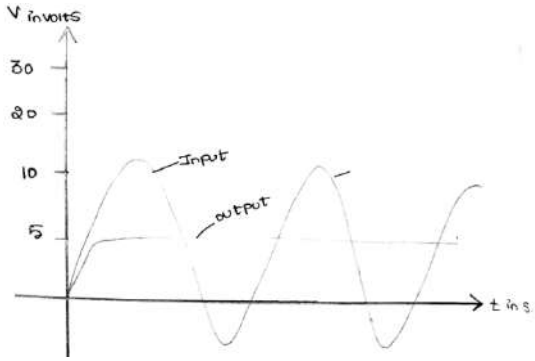
Regulated power supply is an electronic circuit that is designed to provide a constant dc voltage of predetermined value across load terminals irrespective of ac mains fluctuations or load variations.

Regulated linear power supplies are same as the unregulated linear power supply except that a 3-terminal regulator is used in place of the bleeder resistor. Bleeder Resistor is also known as a power supply drain resistor. It is connected across the filter capacitors to drain their stored charge so that the power system supply is not dangerous. The main aim of this supply is to provide the required level of DC power to the load. A regulated power supply generally consists of a step-down transformer, rectifier circuit, and filter circuit and some voltage devise connected to the input. Here the basic circuit diagram for Regulated Linear Power Supply given below.



Simulation Circuit Diagram:





PROCEDURE:

1. Rig up the circuit in PSICE as shown in figure.
2. Go to Analysis> transient> print step: 10ms
   End step:100ms
   V_{OFF}=0 V
   Vamp= 10V
   Frequency=50Hz

3. Click Simulate, a graph window will pop up after simulation is complete, showing the regulated output.