ACS College of Engineering

Approved by AICTE New Delhi, Affiliated to VTU, Belagavi
(A Unit of RajaRajeswari Group of Institutions)
CET Code : E186 COMED-K : E003 PGCET : T918

SelectSmart Activity Report

On

VLSI Front End
By Priya Anathakrishnan
Corporate Technical Trainer

ACTIVITY REPORT

Activity Name & Date	VLSI Front Endon 23-May-2020
Activity Type	Lecture
Conducted By	CTDS Bangalore

About the Activity:

VLSI Design - Verilog Introduction

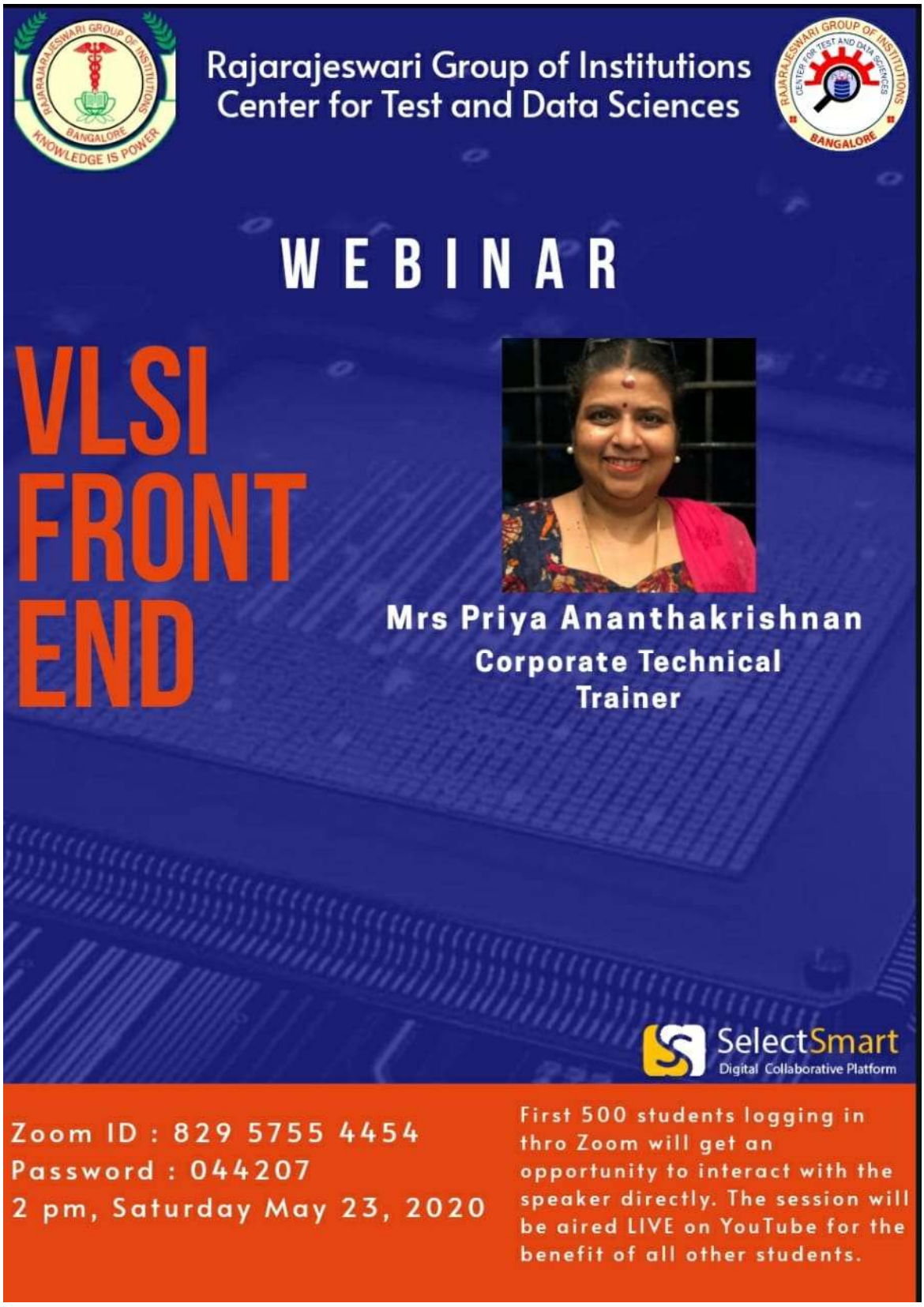
Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using an HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

Presented by Mrs. Priya Ananthakrishnan, Corporate Technical Trainer & Former Senior VLSI Trainer, ChipEdge Technologies Pvt Ltd, Bangalore.

Video Link of the Activity:

https://drive.google.com/file/d/1dCCCP_jQQavUIdIPooOkxZvn_jnY21WT/view?usp=sharing

Invitation:


Rajarajeswari Group of Institutions
Center for Test and Data Sciences
WEBINAR
VLSI FRONT END
Mrs Priya Ananthakrishnan
Corporate Technical Trainer
SelectSmart
Digital Collaborative Platform
Zoom ID : 829 5755 4454
Password : 044207
2 pm, Saturday May 23, 2020
First 500 students logging in thro Zoom will get an opportunity to interact with the speaker directly. The session will be aired LIVE on YouTube for the benefit of all other students.

Mentor Profile:

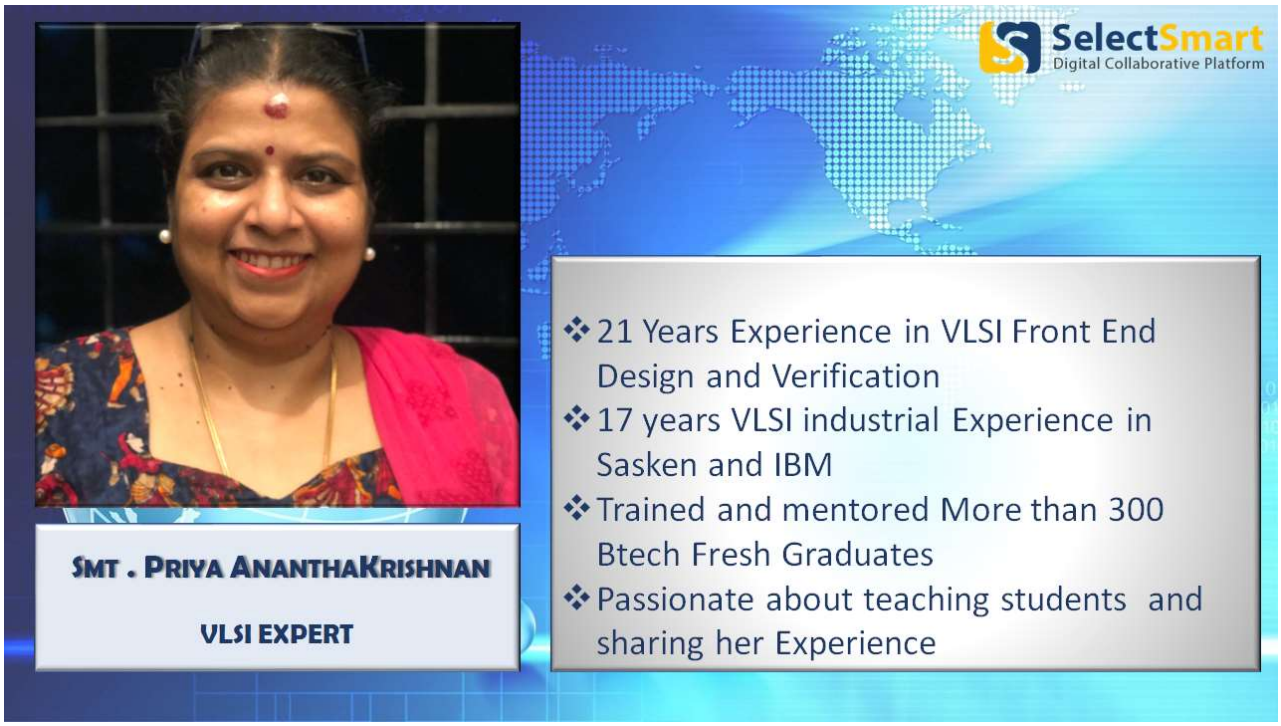


Photo Gallery: