



ACS College of Engineering

Approved by AICTE New Delhi, Affiliated to VTU, Belagavi
(A Unit of RajaRajeswari Group of Institutions)

CET Code : E186 COMED-K : E003 PG CET : T918



SelectSmart Activity Report

On

VLSI Front End

By Priya Anathkrishnan
Corporate Technical Trainer

ACTIVITY REPORT

Activity Name & Date	VLSI Front Endon 23-May-2020
Activity Type	Lecture
Conducted By	CTDS Bangalore

About the Activity:

VLSI Design - Verilog Introduction

Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip-flop. It means, by using an HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

Presented by Mrs. Priya Ananthakrishnan, Corporate Technical Trainer & Former Senior VLSI Trainer, ChipEdge Technologies Pvt Ltd, Bangalore.

Video Link of the Activity:

https://drive.google.com/file/d/1dCCCP_jQQavUldIPooOkxZvn_jnY21WT/view?usp=sharing

Invitation:



Rajarajeswari Group of Institutions
Center for Test and Data Sciences



WEBINAR

VLSI FRONT END



Mrs Priya Ananthakrishnan
Corporate Technical
Trainer



Zoom ID : 829 5755 4454
Password : 044207
2 pm, Saturday May 23, 2020

First 500 students logging in thro Zoom will get an opportunity to interact with the speaker directly. The session will be aired LIVE on YouTube for the benefit of all other students.

Mentor Profile:



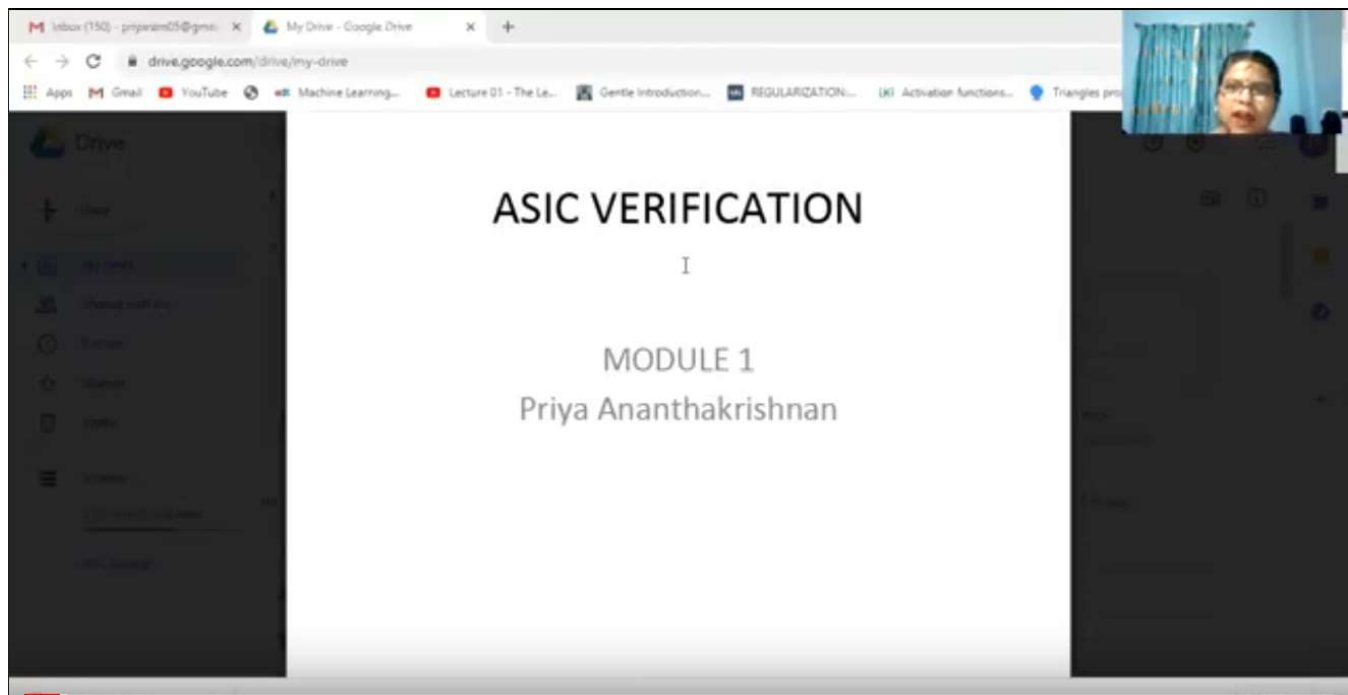
The image shows a professional profile for SMT. Priya Ananthakrishnan, a VLSI expert. It includes a portrait of her on the left, a list of her qualifications and experience on the right, and the SelectSmart logo in the top right corner. The background features a blue world map graphic.

SelectSmart
Digital Collaborative Platform

SMT . PRIYA ANANTHAKRISHNAN
VLSI EXPERT

- ❖ 21 Years Experience in VLSI Front End Design and Verification
- ❖ 17 years VLSI industrial Experience in Sasken and IBM
- ❖ Trained and mentored More than 300 Btech Fresh Graduates
- ❖ Passionate about teaching students and sharing her Experience

Photo Gallery:



The image is a screenshot of a Google Drive presentation slide. The slide content is centered and reads: "ASIC VERIFICATION", "I", "MODULE 1", and "Priya Ananthakrishnan". The browser interface shows the URL "drive.google.com/drive/my-drive" and several open tabs. A small video feed of the presenter is visible in the top right corner of the slide area.

drive.google.com/drive/my-drive

ASIC VERIFICATION

I

MODULE 1

Priya Ananthakrishnan

https://www.youtube.com/watch?v=... My Drive - Google Drive

drive.google.com/drive/my-drive

Machine Learning... Lecture 01 - The Le... Gentle Introduction... REGULARIZATION... Activation functions... Triangles pro

VLSI

Volume (mm³)

Year

Mainframe Workstation Laptop mm-scale sensors

Mini-Computer Personal Computer Smart Phone

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https://www.youtube.com/watch?v=... My Drive - Google Drive

drive.google.com/drive/my-drive

Machine Learning... Lecture 01 - The Le... Gentle Introduction... REGULARIZATION... Activation functions... Triangles pro

VLSI FLOW

Top level: The "idea" or concept

Simulation is performed after each transformation.

Behavioral Description

Behavioral Synthesis

RTL Description (functional verification)

Logic Synthesis

Gate Description

Technology Mapping

Floor Planning

Technology Dependent Network

Layout (timing verification)

Mask Data

Manufacturing

Product

Wafer Sort and Package Test