ACS College of Engineering

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CET Code : E186 COMED-K : E003 PGCET : T918

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On

VLSI Design with Verilog
By Priya Anathakrishnan
Corporate Technical Trainer

ACTIVITY REPORT

Activity Name & Date	VLSI Design with Verilog on 07-June-2020
Activity Type	Lecture
Conducted By	CTDS Bangalore

About the Activity:

VLSI Design - Verilog Introduction

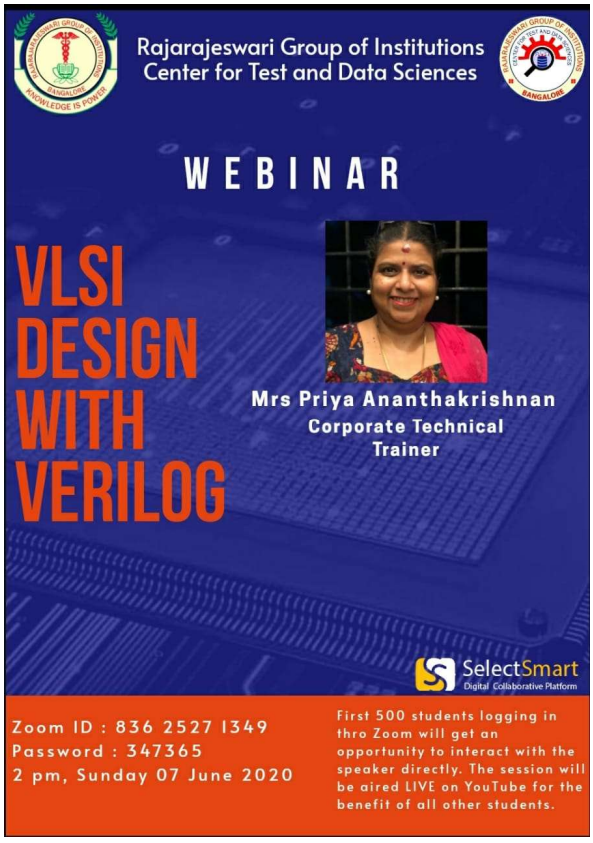
Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using an HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

Presented by Mrs. Priya Ananthakrishnan, Corporate Technical Trainer & Former Senior VLSI Trainer, ChipEdge Technologies Pvt Ltd, Bangalore.

Video Link of the Activity:

https://drive.google.com/file/d/137ZZxVbdkst-h5NnCHLW-0kdsYY_B6Pp/view?usp=sharing

Invitation:



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Mentor Profile:

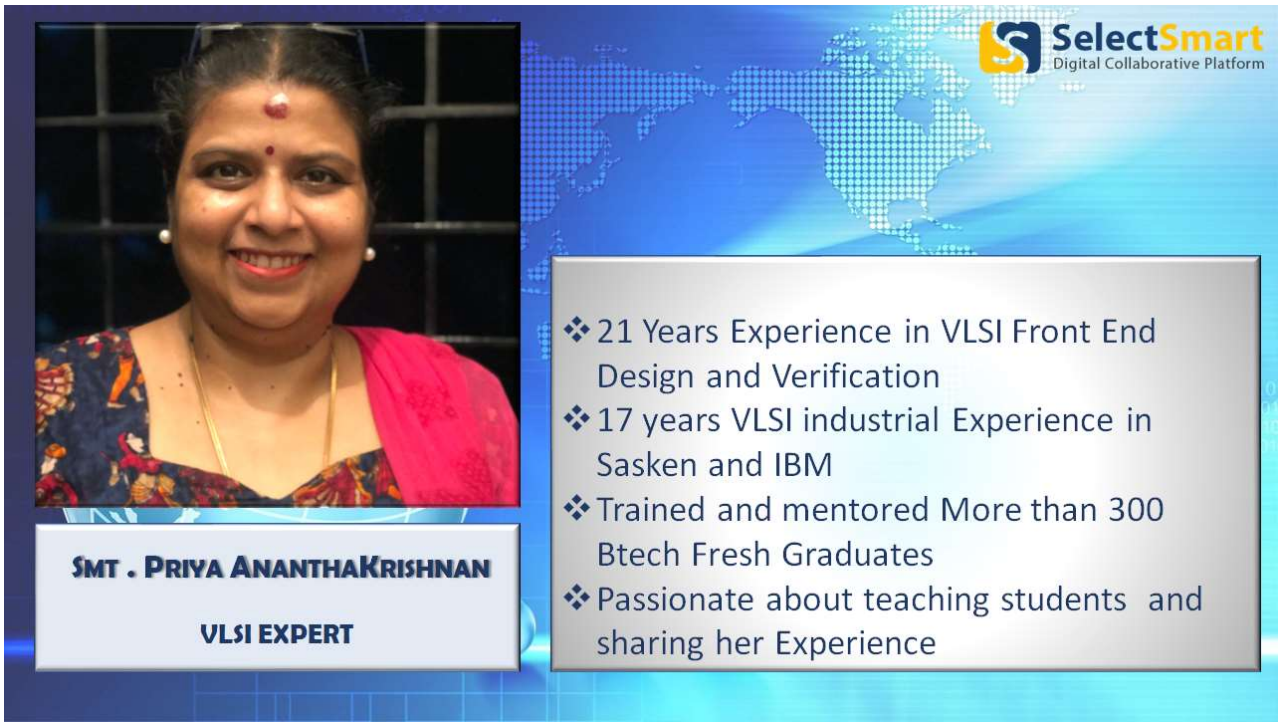

Photo Gallery: