



ACS College of Engineering

Approved by AICTE New Delhi, Affiliated to VTU, Belagavi
(A Unit of RajaRajeswari Group of Institutions)

CET Code : E186 COMED-K : E003 PG CET : T918



SelectSmart Activity Report

On

VLSI Design with Verilog
By Priya Anathakrishnan
Corporate Technical Trainer

ACTIVITY REPORT

Activity Name & Date	VLSI Design with Verilog on 07-June-2020
Activity Type	Lecture
Conducted By	CTDS Bangalore

About the Activity:

VLSI Design - Verilog Introduction

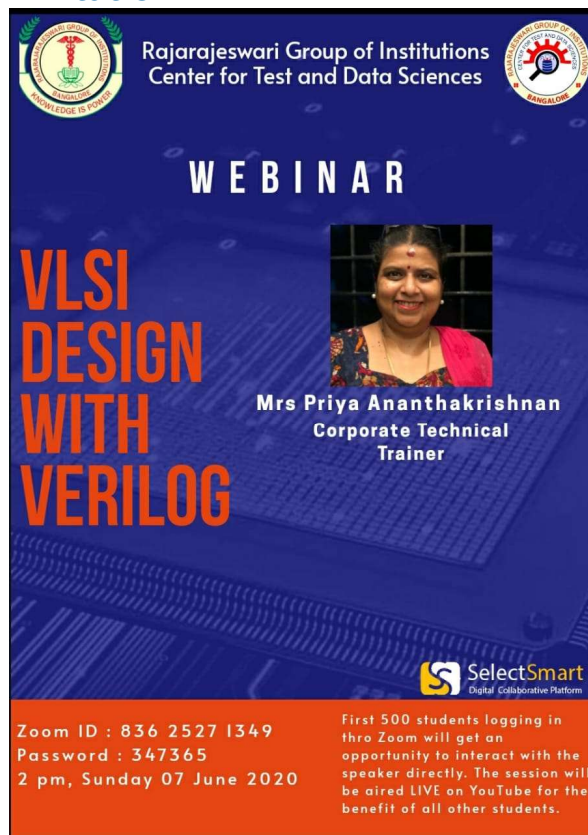
Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip-flop. It means, by using an HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

Presented by Mrs. Priya Ananthakrishnan, Corporate Technical Trainer & Former Senior VLSI Trainer, ChipEdge Technologies Pvt Ltd, Bangalore.

Video Link of the Activity:

https://drive.google.com/file/d/137ZZxVbdkst-h5NnCHLW-0kdsYY_B6Pp/view?usp=sharing

Invitation:



The poster features a dark blue background with a circuit board pattern. At the top left is the logo of Rajarajeswari Group of Institutions with the motto 'KNOWLEDGE IS POWER'. At the top right is the logo of the Center for Test and Data Sciences. The word 'WEBINAR' is written in large white letters. Below it, a photo of Mrs. Priya Ananthakrishnan is shown, with her name and title 'Corporate Technical Trainer' underneath. The main title 'VLSI DESIGN WITH VERILOG' is written in large, bold, orange letters. At the bottom left, the Zoom ID (836 2527 1349) and Password (347365) are listed, along with the date and time: '2 pm, Sunday 07 June 2020'. At the bottom right, the SelectSmart logo is present, along with a note: 'First 500 students logging in thro Zoom will get an opportunity to interact with the speaker directly. The session will be aired LIVE on YouTube for the benefit of all other students.'

Mentor Profile:

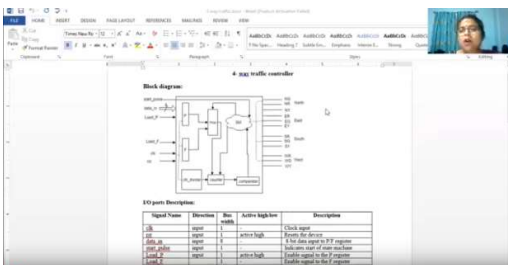
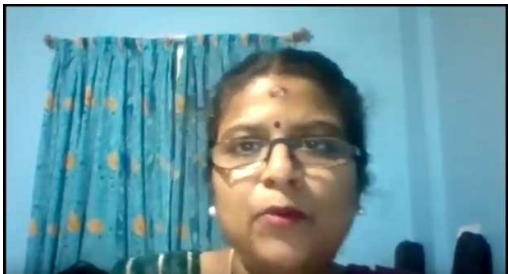


SMT . PRIYA ANANTHAKRISHNAN

VLSI EXPERT

- ❖ 21 Years Experience in VLSI Front End Design and Verification
- ❖ 17 years VLSI industrial Experience in Sasken and IBM
- ❖ Trained and mentored More than 300 Btech Fresh Graduates
- ❖ Passionate about teaching students and sharing her Experience

Photo Gallery:



Signal Name	Direction	Bus Width	Active Logic	Description
clk	input	1	clock	Clock signal
en	input	1	enable	Enable for logic
en0	input	1	enable	Enable for logic
en1	input	1	enable	Enable for logic
en2	input	1	enable	Enable for logic
en3	input	1	enable	Enable for logic
en4	input	1	enable	Enable for logic
en5	input	1	enable	Enable for logic
en6	input	1	enable	Enable for logic
en7	input	1	enable	Enable for logic

