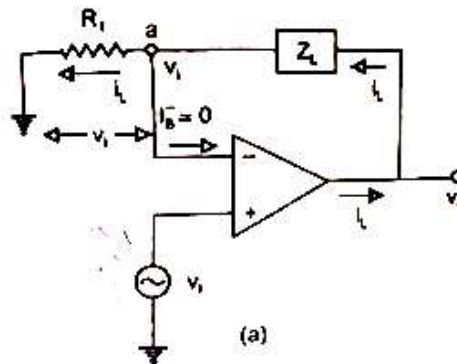


Module-2

V - I and I - V Converter:

Draw the circuit of a Voltage to Current converter with a Floating load. Explain the operation.



Here, the load Z_L is floating. Voltage at node 'a' is V_i because of virtual short ($v_d = 0$).

$$V_i = i_i R_1$$

but

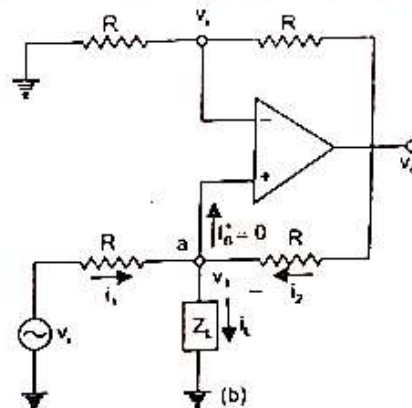
$$i_i = i_L \quad \text{since } I_b = 0.$$

Therefore, Eqn (1) can be written as

$$i_L = \frac{v_i}{R_1}$$

That is the input voltage v_i is converted into an output current of v_i/R_1 .

Draw the circuit of a Voltage to Current converter with a Grounded load. Explain the operation.



Here, the load Z_L is grounded. Let v_1 be the voltage at node 'a'.

Writing KVL, we get

$$i_1 + i_2 = i_L$$

$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L \quad \text{or}$$

$$v_i + v_o - 2v_1 = i_L R$$

$$v_1 = \frac{v_i + v_o - i_L R}{2}$$

Since the op-amp is used in non-inverting mode, the voltage gain of the non-inverting amplifier circuit is

$$A_v = \frac{v_o}{v_1} = 1 + \frac{R}{R} = 2 \quad \text{or}$$

$$v_o = 2v_1 = 2 \frac{v_i + v_o - i_L R}{2} \quad \text{or}$$

$$v_o = v_i + v_o - i_L R \quad \text{or}$$

$$v_i = i_L R \quad \text{or}$$

$$i_L = \frac{v_i}{R}$$

That is the input voltage v_i is converted into an output current of v_i/R_1 .

Applications:

- i) Low voltage dc and ac voltmeter
- ii) LED Tester
- iii) Zener Diode Tester.

Op-amp circuits using Diodes:

Rectifiers:

an electrical element which does not have a linear relationship between current & voltage. It is a non-linear element.

Discuss the advantages of a precision rectifier over an ordinary rectifier.

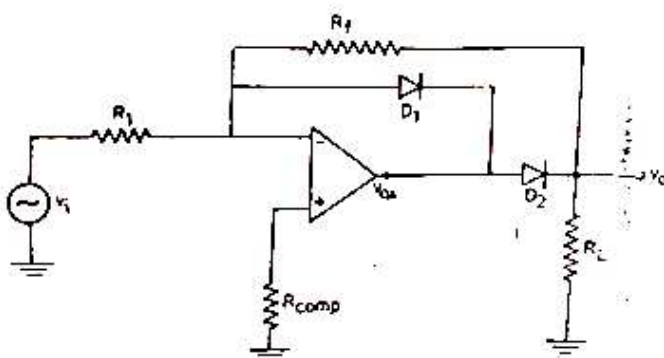
Rectifiers are implemented using non-linear devices such as diodes. The major limitation of ordinary diode is that it cannot rectify voltages below V_f (~ 0.7 V). The non-zero forward voltage drop V_f of a practical diode may cause intolerable errors in low level signal rectification. This shortcoming is avoided by placing the diode inside the negative feedback path of an op-amp. With this, the forward voltage drop can be eliminated to give precision rectification. Hence op-amp rectifiers are called precision rectifiers or small signal rectifiers.

The advantages of precision rectifiers over simple diode rectifiers are as follows:

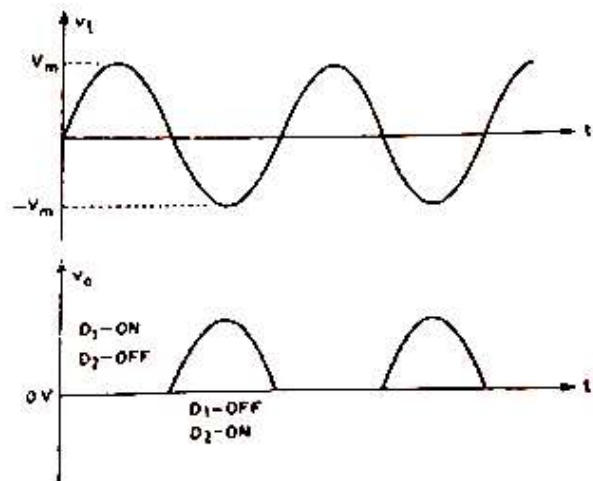
1. No diode voltage drop between input and output
2. The ability to rectify very small voltages (< 0.7 V)
3. Amplification if required
4. Low output impedance.

Sketch the circuit of a precision Half Wave Rectifier. Draw the input and output waveforms and explain the circuit operation.

Circuit diagram:

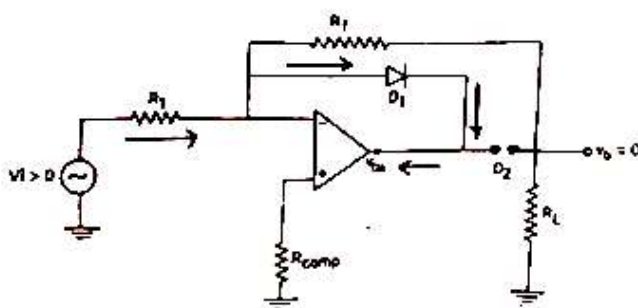


I/O Waveforms:



The precision HWR uses an inverting amplifier configuration.

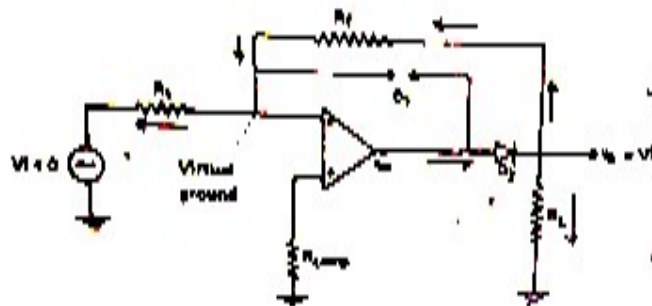
For, $V_i > 0$



During the positive half cycle of the input, the op-amp output terminal V_{OA} goes negative, causing D_2 to be reverse biased and D_1 to be forward biased. The op-amp's output voltage V_{OA} goes negative by one diode drop. Without D_1 in the circuit, the op-amp output would be driven to $-V_{sat}$. The purpose of D_1 is to keep the op-amp output from going into saturation. The output voltage is zero.

$$v_o = 0 \text{ and } v_{OA} = -0.7V$$

For, $V_i < 0$



During the negative half cycle of the input, the op-amp output terminal V_{OA} goes positive, causing D_1 to be reverse biased and D_2 to be forward biased. While D_2 is forward biased, the circuit functions as an inverting amplifier circuit to give an output

$$V_o = -\frac{R_f}{R_i}(-V_i)$$

With $R_f = R_i$, the circuit acts like an inverter.

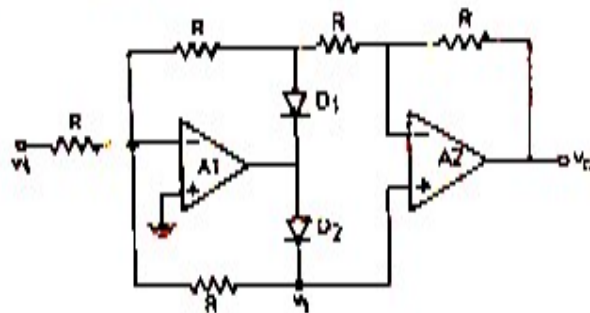
Therefore, $V_o = -V_i$

Thus, the positive half cycle is clipped off and the negative half cycle of the input is inverted.

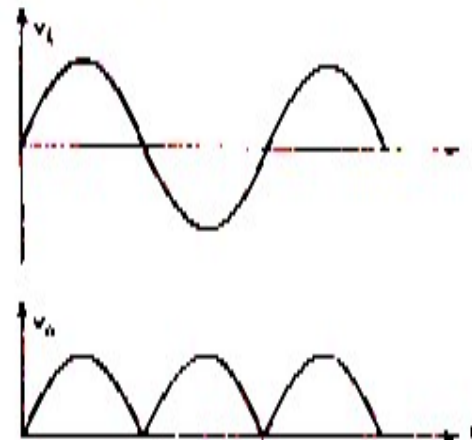
If $R_f > R_i$, the output is an amplified version of the input.

Sketch the circuit of a precision Full Wave Rectifier. Draw the input and output waveforms and explain the circuit operation.

Circuit diagram:

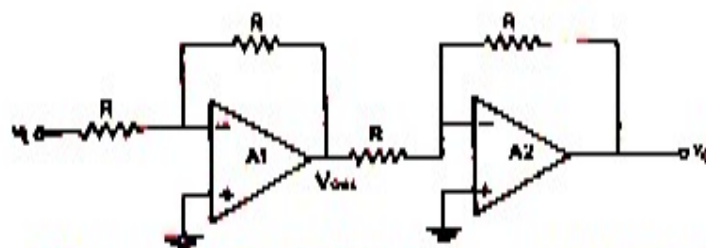


I/O Waveforms:



A precision full wave rectifier is also known as an Absolute value circuit. This means the circuit output is the absolute value of the input peak voltage regardless of the input polarity.

For, $V_i > 0$



During the positive half cycle of the input, the op-amp A_1 output terminal V_{OA1} goes negative, causing D_1 to be reverse biased and D_2 to be forward biased. Both the op-amps A_1 and A_2 act as inverter as shown in equivalent circuit.

$$V_{OA1} = -V_i$$

$$V_o = -V_{OA1} = -(-V_i)$$

$$V_o = V_i$$

For, $V_i < 0$:

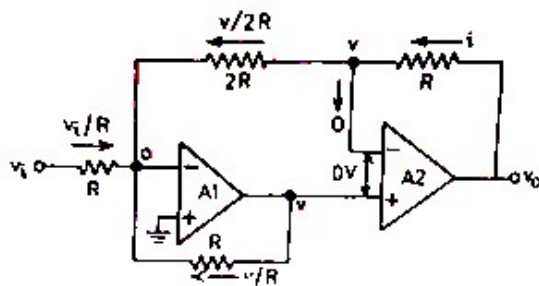
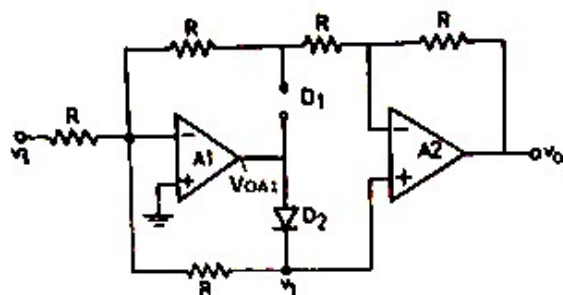


Fig a

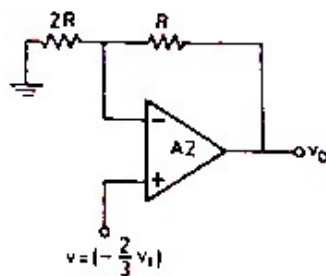


Fig b

During the negative half cycle of the input, the op-amp A_1 output terminal V_{OA1} goes positive, causing D_1 to be reverse biased and D_2 to be forward biased. The equivalent circuit is shown in Fig a.

Let the output voltage of op-amp A_1 be ' v '. Because of virtual short ($v_d = 0$) at op-amp A_2 , the inverting input terminal of op-amp A_2 is also at voltage ' v '.

Applying KCL at node ' a ' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0 \text{ or}$$

$$v = -\frac{2}{3}v_i$$

But $v_i < 0$

Therefore,

$$v = -\frac{2}{3}(-v_i)$$

$$v = \frac{2}{3}v_i \text{(1)}$$

The equivalent circuit of Fig a is a non-inverting amplifier as shown in Fig b.

The output voltage v_o is

$$v_o = \left(1 + \frac{R}{2R}\right)v$$

$$v_o = \left(1 + \frac{1}{2}\right)\left(\frac{2}{3}v_i\right)$$

$$v_o = \left(\frac{3}{2}\right)\left(\frac{2}{3}v_i\right)$$

$$v_o = v_i$$

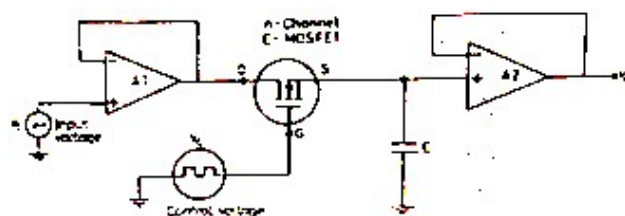
where V_{GS} is the gate voltage and μ_n is the conductivity of the channel.

Sample and Hold Circuit:

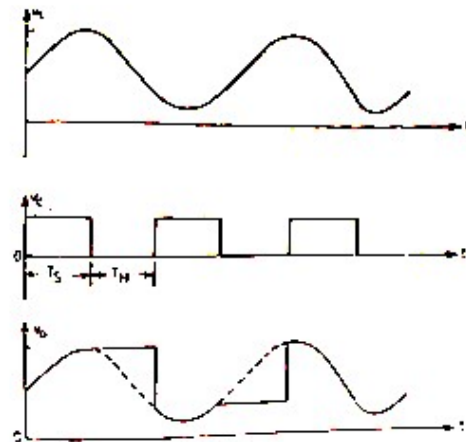
Sketch the op-amp Sample and Hold circuit, draw the Signal, Control and Output voltage waveforms and explain the circuit operation.

A sample and hold circuit samples instantaneous amplitudes of an analog signal voltage at any point in its waveform and holds the voltage level constant until the next sample is acquired.

Circuit Diagram:



Voltage Waveforms:



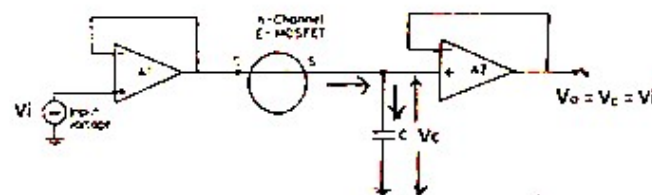
Operation:

The n-channel E - MOSFET switch is included to alternately connect and disconnect the capacitor at the output of op-amp A₁. The analog signal V_i to be sampled is applied to the drain of E-MOSFET. The MOSFET switch is repeatedly switched ON and OFF by the pulse waveform called the control voltage V_c. The control voltage V_c is applied to the gate of E-MOSFET.

The frequency of the control voltage V_c should be kept higher than (at least twice) the input so as to retrieve the input from output waveform.

$$f_c \geq 2f_i$$

When v_c is positive:



When the control voltage v_c is positive, the E-MOSFET turns ON and the capacitor C charges to the instantaneous value of input v_i with a time constant

$$[R_o + r_{DS(on)}]C$$

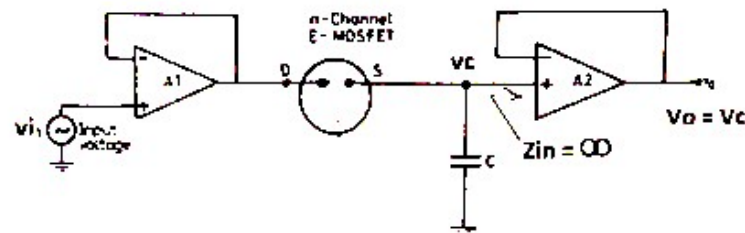
where R_o is the output resistance of the Voltage follower A_1 and

$r_{DS(on)}$ is the resistance of the MOSFET when ON

Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2 .

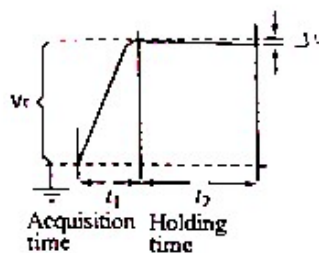
$$V_o = V_C = V_i$$

When v_c is zero:



During the time when control voltage v_c is zero, the E-MOSFET is OFF. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it.

$$V_o = V_C$$



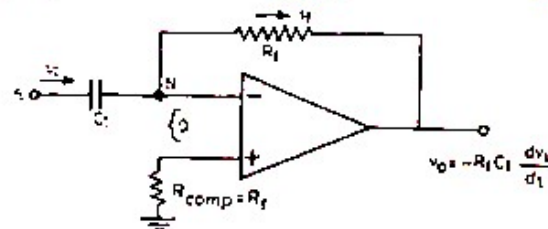
Acquisition time t_1 : The time period t_1 , during which voltage across the capacitor is equal to input voltage is called acquisition time or sample period.

Holding time t_2 : The time period t_2 of v_c during which the voltage across the capacitor is held constant is called holding time or hold period.

Differentiator:

Draw the circuit diagram of basic Op-amp Differentiator. Derive an equation for the output voltage.

Differentiator circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform.



The node N is at virtual ground potential i.e., $v_N = 0$. The current i_C through the capacitor is

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{d}{dt}(v_i - 0) = C_1 \frac{dv_i}{dt}$$

The current i_f through the feedback resistor is

$$i_f = \frac{v_N - v_o}{R_f} = \frac{0 - v_o}{R_f} = -\frac{v_o}{R_f}$$

Therefore, the nodal equation at node N is,

$$i_C = i_f + i_{in}$$

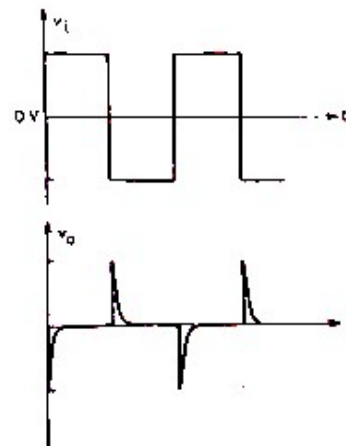
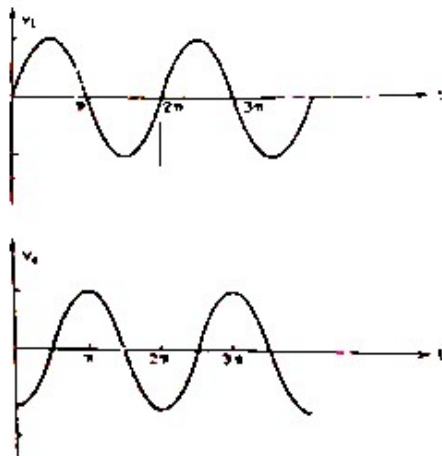
$$i_C = i_f \quad \text{since } i_{in} = 0$$

$$C_1 \frac{dv_i}{dt} = -\frac{v_o}{R_f}$$

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

Thus, the output voltage v_o is a constant $(-R_f C_1)$ times the derivative of the input voltage v_i . $R_f C_1$ is the time constant of the differentiator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal v_i .

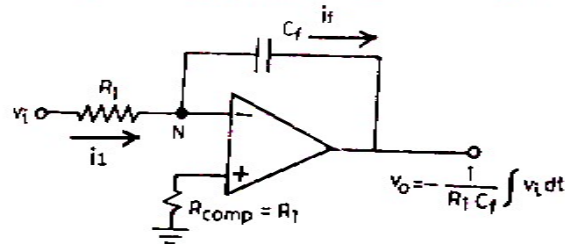
I/O Waveforms:



Integrator:

Draw the circuit diagram of basic Op-amp Integrator. Derive an equation for the output voltage.

Integrator circuit performs the mathematical operation of integration, that is, the output waveform is the integration of input waveform.



The node N is at virtual ground potential i.e., $v_N = 0$. The current i_f through the capacitor C_f is

$$i_f = C_f \frac{d}{dt}(v_N - v_o) = C_f \frac{d}{dt}(0 - v_o) = -C_f \frac{dv_o}{dt}$$

The current i_i through the resistor R_i is

$$i_i = \frac{v_i}{R_i}$$

Therefore, the nodal equation at node N is,

$$i_1 = i_f + i_R$$

$$i_1 = i_f \quad \text{since } i_R = 0$$

$$\frac{v_i}{R_1} = -C_f \frac{dv_o}{dt}$$

$$\frac{dv_o}{dt} = -\frac{1}{R_1 C_f} v_i$$

Integrating both sides, we get

$$\int_0^t dv_o = -\frac{1}{R_1 C_f} \int_0^t v_i dt$$

$$v_o(t) = -\frac{1}{R_1 C_f} \int_0^t v_i(t) dt + v_o(0)$$

where $v_o(0)$ is the initial output voltage

Thus, the output voltage v_o is a constant $(-1/R_1 C_f)$ times the integral of the input voltage v_i . $R_1 C_f$ is the time constant of the integrator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal v_i .

For good integration, one must ensure that the time period T of the input signal is smaller than or equal to $R_1 C_f$.

$$T \leq R_1 C_f$$

I/O Waveforms:

