BIOMEMS Module -5

Microsystem Fabrication Process

1. Photolithography,
2. Ion Implantation,
3. Diffusion,
4. Oxidation,
5. Chemical Vapour Deposition,
6. Physical Vapour Deposition,
7. Deposition By Epitaxy,
8. Etching,
9. The LIGA Process,
10. Design Consideration Overview,
11. Design Constraints.

(Text 1: 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.9, 9.4, 10.2, 10.2.1)

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Microsystems Fabrication Processes

To fabricate any solid device component, one must first select materials and adequate fabrication method.

For MEMS and microsystems components, the sizes are so small that no machine tools, e.g. lathe, milling machine, drilling press, etc. can do the job. There is simply no way one can even grip the work piece.

Consequently, radically different techniques, non-machine-tool techniques need to be used for such purpose.

Most physical-chemical processes developed for "shaping" and fabricating ICs are adopted for microsystems fabrications. This is the principal reason for using silicon and silicon compounds for most MEMS and microsystems – because these are the materials used to produce ICs.

Microfabrication

by physical-chemical processes

Traditional Manufacturing by machine tools

Microfabrication Processes

- Photolithography
- Ion implantation
- Diffusion
- Oxidation
- Chemical vapor deposition
- Physical vapor deposition (Sputtering)
- Deposition by expitaxy
- Etching

Photolithography

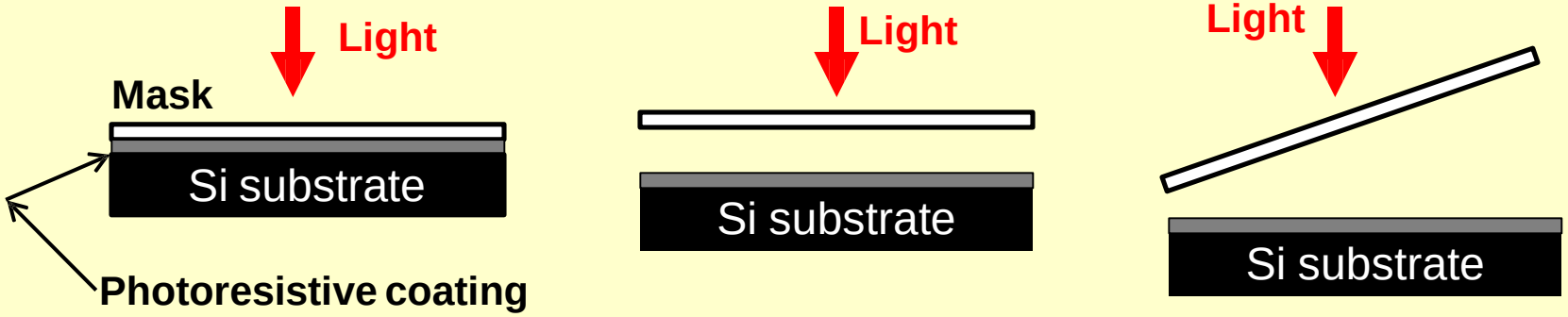
Photolithography process involves the use of an optical image and a photosensitive film to produce desired patterns on a substrate.

The "optical image" is originally in macro scale, but is photographically reduced to the micro-scale to be printed on the silicon substrates.

The desired patterns are first printed on light-transparent mask, usually made of quartz.

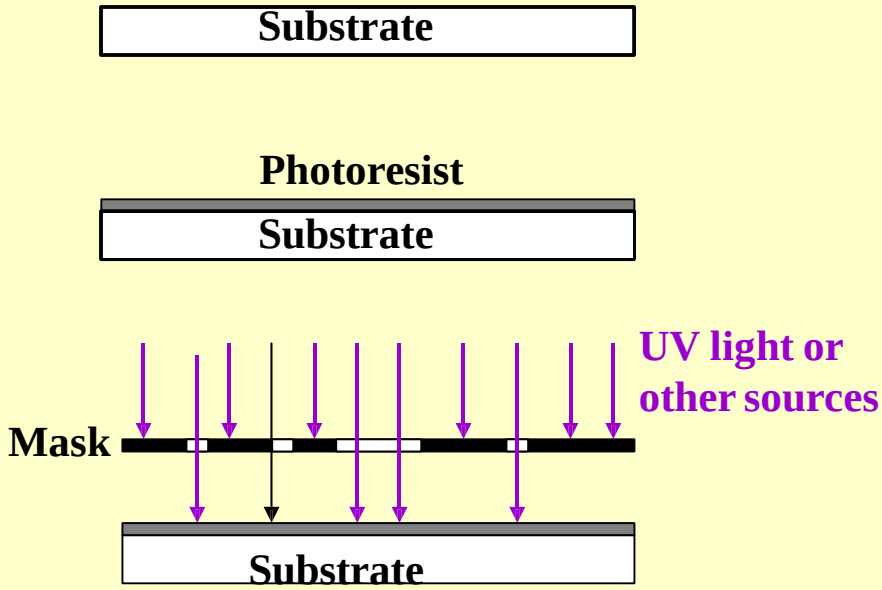
The mask is then placed above the top-face of a silicon substrate coated with thin film of photoresistive materials.

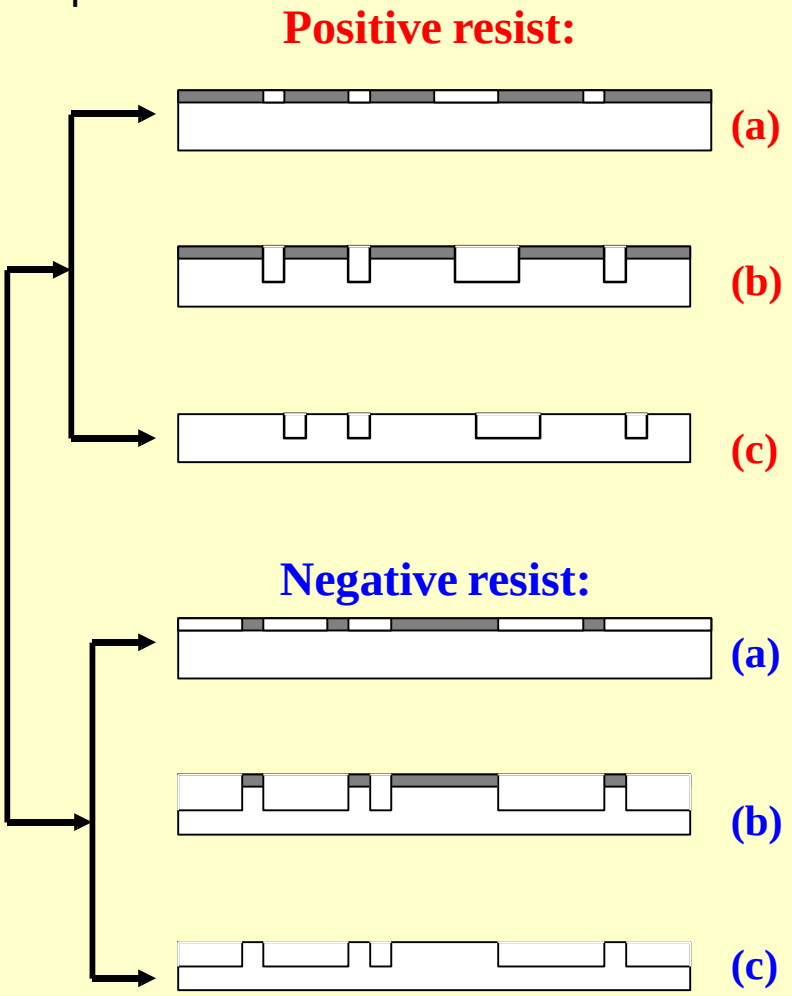
The mask can be in contact with the photoresistave material, or placed with a gap, or inclined to the substrate surface:



Photolithography-Cont'd

A positive photoresist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. The unexposed portion of the photoresist remains insoluble to the photoresist developer





Processes:

(a) Development
(b) Etching
(c) Photoresist removal

A negative photoresist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer.

Photolithography- Cont'd

The two kinds of photoresists:

- **Positive resists:**

There are two kinds of positive resists:
(1) the **PMMA** (polymethymethacrylate) resists,
(2) the **two-component DQN resist** involving diazoquinone ester (DQ) and phenolic novolak resin (N).

In the latter kind, the first component takes about 20-50% by weight in the compound.

Positive resists are sensitive to UV lights with the maximum sensitivity at a wavelength of 220 nm.

The PMMA resists are also used in photolithography involving electron beam, ion beam and x-ray. Most positive resists can be developed in alkaline solvents such as KOH (potassium peroxide), TMAH (tetramethylammonium hydroxide), ketones or acetates.

Photolithography- Cont'd

- **Negative resists:**

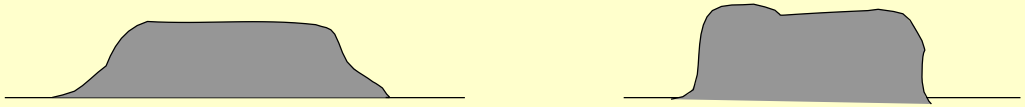
(1) Two-component bis (aryl) azide rubber resists, and
(2) Kodak KTFR (azide-sensitized polyisotroprene rubber).

Negative resists are less sensitive to optical and x-ray exposures but more sensitive to electron beams.

Xylene is the most commonly used solvent for developing negative resists.

Line definitions of photoresists:

In general, positive resists provide more clear edge definitions than the negative resists. So, it is a better option for high resolution patterns for micro devices.



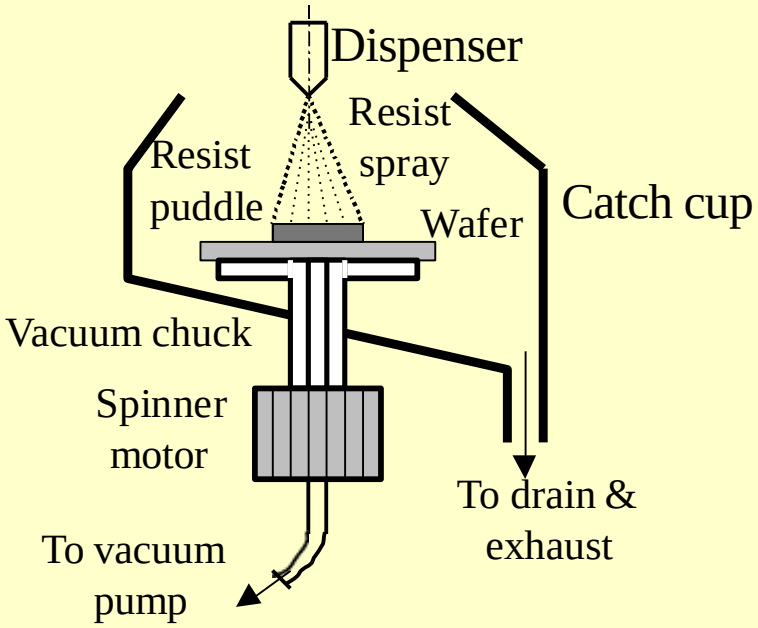
(a) by negative resists

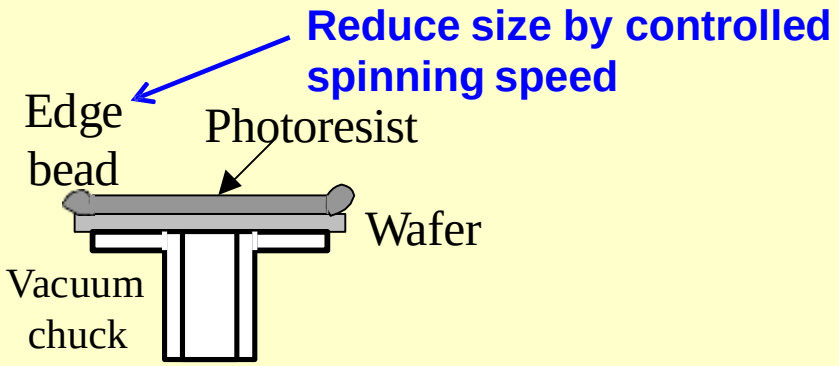
(b) by positive resists

Photolithography- Cont'd

Application of photoresists

- The process begins with securing the substrate wafer onto the top of a vacuum chuck.
- A resist puddle is first applied to the center portion of the wafer from a dispenser.
- The wafer is then subjected to high speed spinning at a rotational speed from 1500 to 8000 rpm for 10 to 60 seconds. The speed is set depending on the type of the resist, the desired thickness and uniformity of the resist coating.
- The centrifugal forces applied to the resist puddle cause a uniform spread of the fluid over the entire surface of the wafer.
- Typically the thickness is between 0.5 – 2 μm with ±5 nm variation.
  For some microsystems applications, the thickness had been increased to 1 cm.





Photolithography- Cont'd

Light sources

Photoresist materials used in micro fabrication are sensitive to light with wavelength ranging from 300 to 500 nm.

Most popular light source for photolithography is the mercury vapor lamps. This light source provides a wavelength spectrum from 310 to 440 nm.

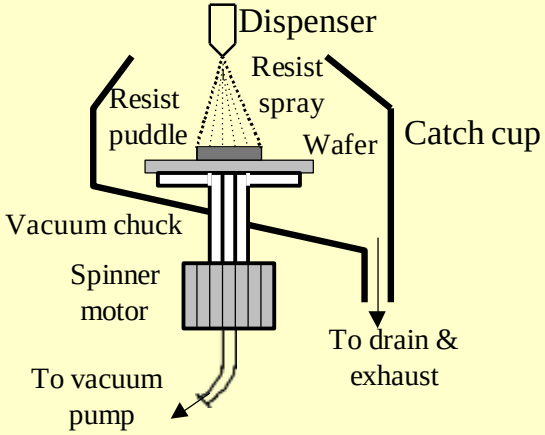
Deep UV (ultra violet) light has a wavelength of 150-300 nm and the UV light source has wavelengths between 350-500 nm.

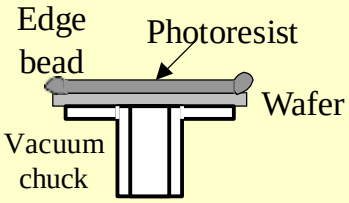
In special applications for extremely high resolutions, x-ray is used. The wavelength of x-ray is in the range from 4 to 50 Angstrom. (an Angstrom, = 0.1 nm or 10^{-4} μm).

Photolithography- ends

Photoresist development

- The same spinner may be used for development after exposure with dispensing development solvent.
- A rising distilled water follow the development.
- Developers agent for +ve resistor are KOH or TMAH. Xylene is the agent for –ve resistors,



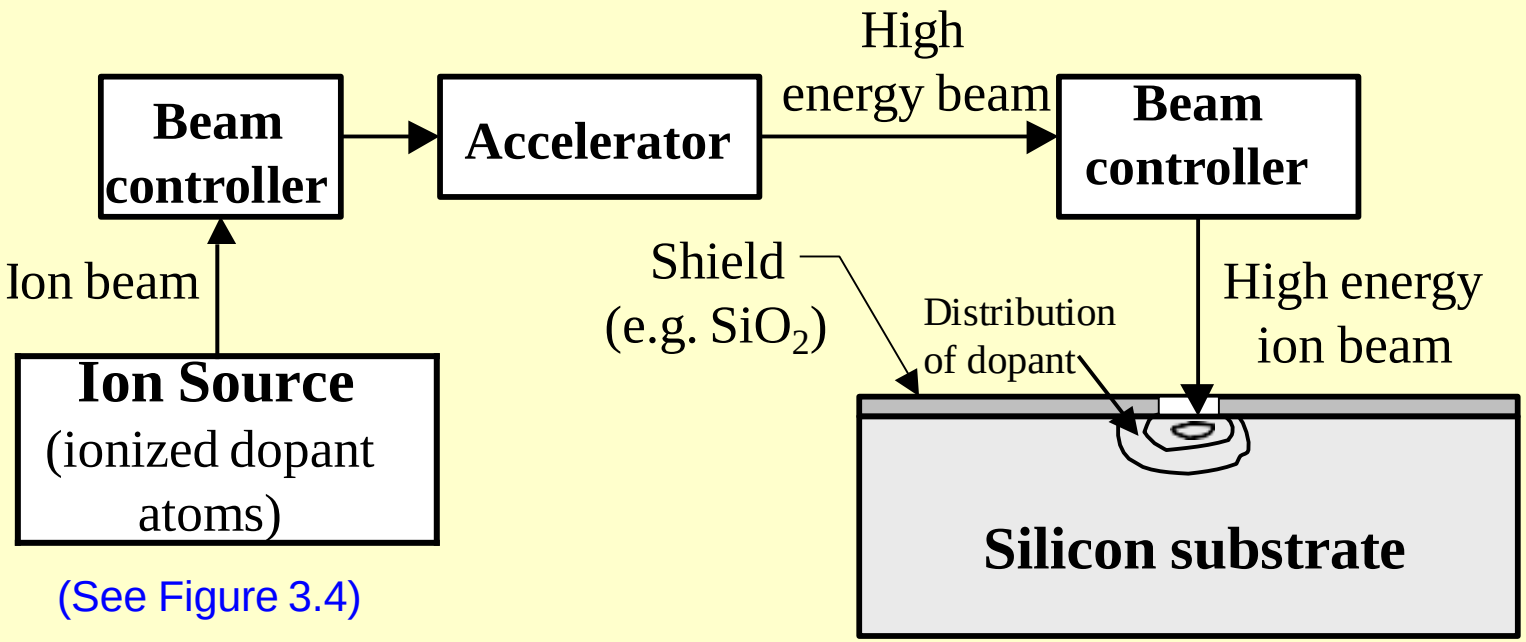


Photoresist removal and postbaking

- After development and the desired pattern in created in the substrate, a descumming process takes place.
- The process uses O_2 plasma to remove the bulk of photoresist.
- Postbaking to remove the residue of solvent at 120°C for 20 minutes.
- Etching will remove all residue photoresist.

Ion Implantation

- It is physical process used to dope silicon substrates.
- It involves "forcing" free charge-carrying ionized atoms of B, P of As into silicon crystals.
- These ions associated with sufficiently high kinetic energy will be penetrated into the silicon substrate.
- Physical process is illustrated as follows:



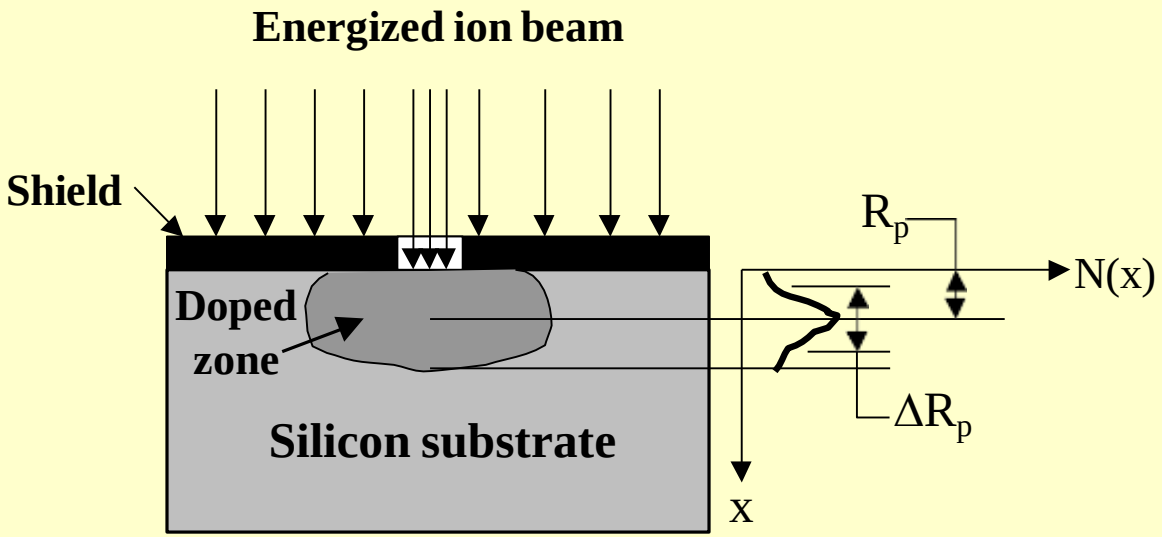
(See Figure 3.4)

Required energy for ion implantation:

Dopants	p- or n-type	Ionization Energy (eV)
Phosphorus (P)	**n**	**0.044**
Arsenic (As)	**n**	**0.049**
Antimony (Sb)	n	0.039
Boron (B)	**p**	**0.045**
Aluminum (A<)	p	0.057
Gallium (Ga)	p	0.065
Indium (In)	p	0.160

Ion Implantation – Cont'd

Density distribution in depth



$$N(x) = \frac{Q}{\sqrt{2\pi}\Delta R_p} \exp\left[\frac{-(x - R_p)^2}{2\Delta R_p^{\,2}}\right] \qquad (8.1)$$

where R_p = projected range in μm,
ΔR_p = scatter or "straggle" in μm, and
Q = dose of ion beam (atoms/cm^2)

Ion Implantation – Cont'd

Density distribution in depth – Cont'd

(a) At 30 KeV energy level:

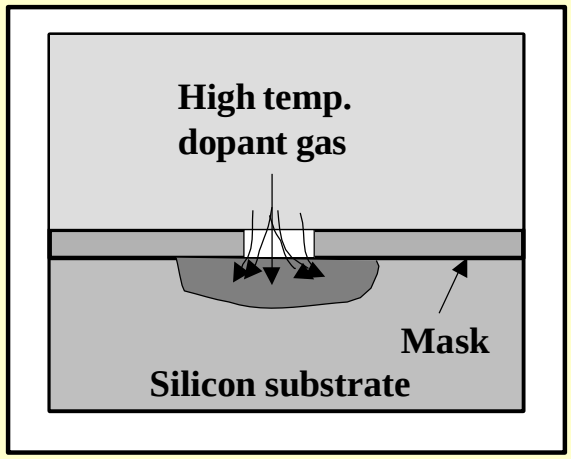
Ion	Range, R_p (nm)	Straggle, ΔR_p (nm)
Boron (B)	106.5	39.0
Phosphorous (P)	42.0	19.5
Arsenic (As)	23.3	9.0

(b) At 100 KeV energy level:

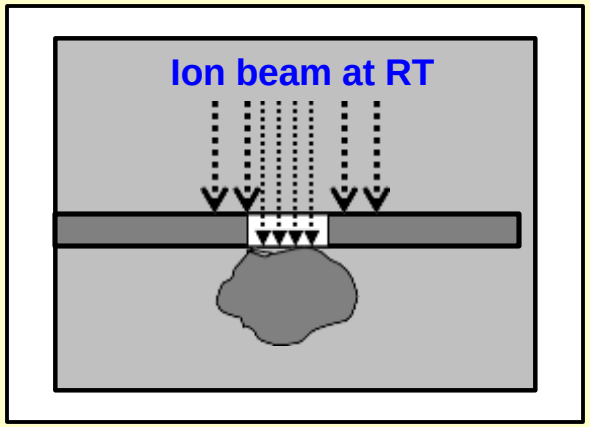
Ion	Range, R_p (nm)	Straggle, ΔR_p (nm)
Boron (B)	307.0	69.0
Phosphorous (P)	135.0	53.5
Arsenic (As)	67.8	26.1

Diffusion

- Diffusion is another common technique for doping silicon substrates.
- Unlike ion implantation, diffusion takes place at high temperature.
- Diffusion is a chemical process.
- The profile of the spread of dopant in silicon by diffusion is different from that by ion implantation:



Dopant profile by Diffusion



Dopant profile by ion implantation

Diffusion – Cont'd

Design analysis of diffusion

Fick's law governs diffusion (Chapter 3)**:**

$$F = -D\frac{\partial N(x)}{\partial x} \qquad (8.2)$$

where F = Dopant flux, which is the number of dopant atoms passing through a unit area of the substrate in a unit time (atoms/cm^2-sec)
D = Diffusion coefficient or diffusivity of the substrate to the dopant (cm^2/sec)
N = Dopant concentration in the substrate per unit volume. (atoms/cm^3)

The distribution of dopant, N(x,t) in the "depth" direction of the substrate at time t is obtained from the "Diffusion equation":

$$\frac{\partial N(x,t)}{\partial t} = D\frac{\partial^2 N(x,t)}{\partial x^2} \qquad (8.3)$$

Diffusion – Cont'd

Solution of diffusion equation

$$\frac{\partial N(x,t)}{\partial t} = D\frac{\partial^2 N(x,t)}{\partial x^2} \qquad (8.3)$$

Initial condition *(t = 0):*

N(x,0) = 0, **meaning there is no impurity in the substrate when the diffusion process begins.**

Boundary conditions *(at x = 0 and ∞):*

$N(0,t) = N_s$, **which is the concentration at the surface exposed to the gaseous dopant.**

$N(\infty, t) = 0$, **meaning the diffusion of foreign substance is highly localized, and that the concentration far away from the contacting surface is negligible.**

The solution of the diffusion equation in (8.3) with these conditions is:

$$N(x,t) = N_s\, erfc\left(\frac{x}{2\sqrt{Dt}}\right) \qquad (8.4)$$

where erfc(x) is the complementary error function that has the form:

$$erfc(x) = 1 - erf(x) = 1 - \frac{2}{\sqrt{\pi}}\int_0^x e^{-y^2} dy \qquad (8.5)$$

Diffusion – Cont'd

The diffusivity, D:

The diffusivity of silicon with common dopants can be obtained by an empirical formula:

$$\ln(\sqrt{D}) = aT' + b \qquad (8.6)$$

in which the temperature, T' = 1000/T with T = diffusion temperature in K.

The constants a and b for common dopants can be obtained from:

Dopants	Constant, a	Constant, b
Boron	-19.9820	13.1109
Arsenic	-26.8404	17.2250
Phosphorus ($N_s = 10^{21}/cm^3$)	-15.8456	11.1168
Phosphorus ($N_s = 10^{19}/cm^3$)	-20.4278	13.6430

Example 8.2

A silicon substrate is subjected to diffusion of boron dopant at 1000°C with a dose $10^{11}/cm^2$. Find:

(a) the expression for estimating the concentration of the dopant in the substrate,

(b) the concentration at 0.1 μm beneath the surface after one hour into the diffusion process. The substrate is initially free of impurity.

Solution:

First, to find the diffusivity, D with temperature **T' = 1000/(1000+273)** = 0.7855.
From the Table, we have constants, **a = -19.982** and **b = 13.1109**.
Thus, **D** is: 0.005676 $\mu m^2/h$ = **1.5766×10^{-6} $\mu m^2/s$**, which is in a "ball park" agreement with that from Figure 3.12 on P. 95

(a) Since initially N(x,0) = 0, and N(0,t) = Ns = 10^{11} atoms/cm^2, and N(∞,t) = 0, from Eq. (8.4), we have:

$$N(x,t) = N_s\, erfc\left(\frac{x}{2\sqrt{Dt}}\right) = 10^{11}\, erfc\left(\frac{x}{2\sqrt{1.5766 \times 10^{-6}\, t}}\right) = 10^{11}\, erfc\left(\frac{398.21x}{\sqrt{t}}\right)$$

$$N(x,t) = 10^{11}\left(1 - erf\left(\frac{398.21x}{\sqrt{t}}\right)\right)$$

Example 8.2 – cont'd

(b) For x= 0.1 μm at t = 1 h, or 3600 seconds into the diffusion, the concentration is:

$$N(0.1\mu m, 1hour) = 10^{11}\left[1 - erf\left(\frac{398.21x0.1}{\sqrt{3600}}\right)\right] = 10^{11}\left[1 - erf\,(0.6637)\right]$$

$$= 10^{11}(1 - 0.6518) = 3.482x10^{10}/cm^3$$

The numerical value of the error function, erf (0.6637) is obtained from Figure 3.14 on P. 96

Oxidation

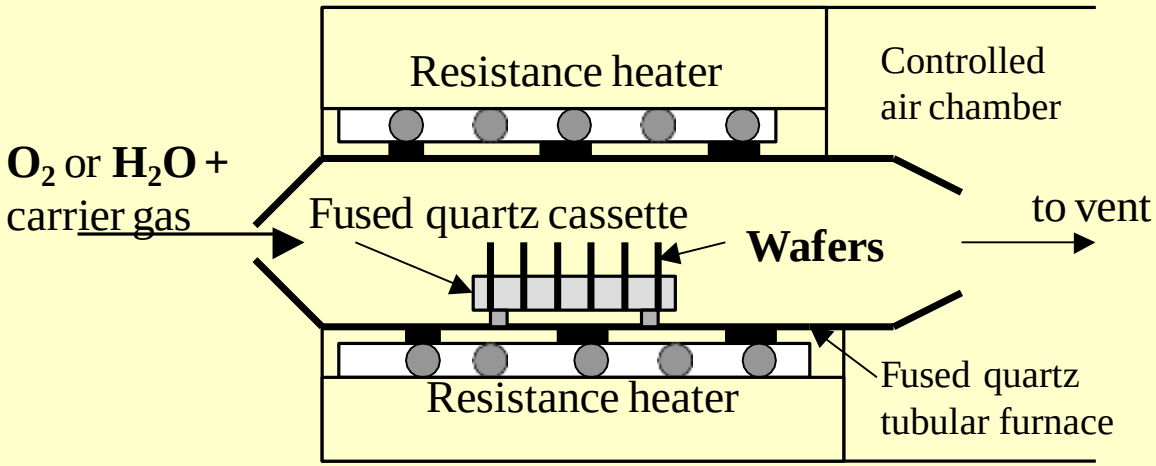
SiO_2 is an important element in MEMS and microsystems. Major application of SiO_2 layers or films are:

(1) To be used as thermal insulation media
(2) To be used as dielectric layers for electrical insulation

- **SiO_2 can be produced over the surface of silicon substrates either by:**
  (1) Chemical vapor deposition (CVD), or
  (2) Growing SiO_2 with dry O_2 in the air, or wet steam by the following two chemical reactions at high temperature:

$$Si\ (solid) + O_2\ (gas) \rightarrow SiO_2\ (solid)$$

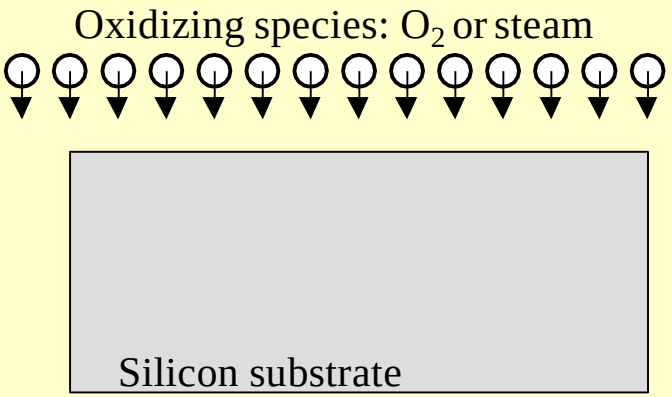
$$Si\ (solid) + 2H_2O\ (steam) \rightarrow SiO_2\ (solid) + 2H_2\ (gas)$$



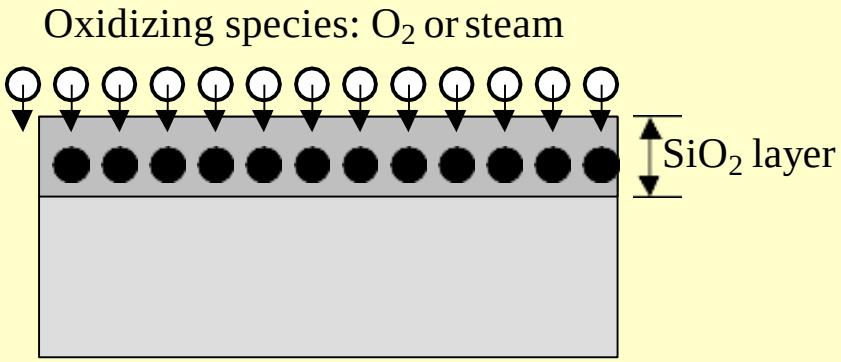
Oxidation – Cont'd

Principle of thermal oxidation:

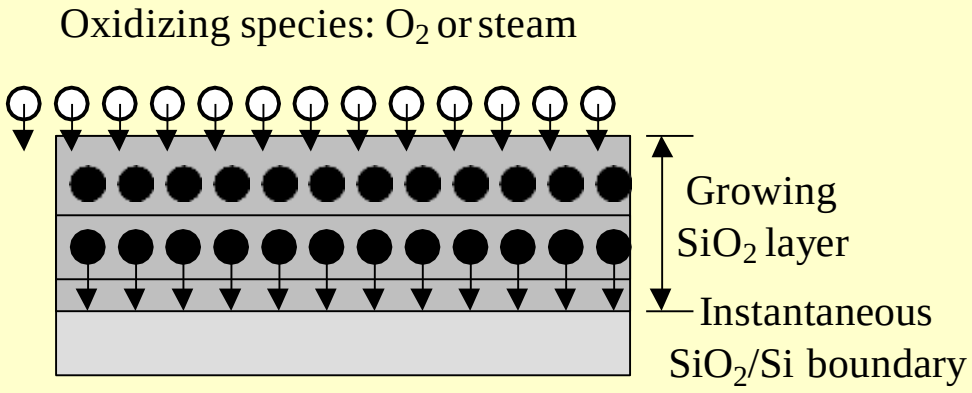
It is a combined <u>continuous</u> physical diffusion and chemical reactions



(1) At the inception of oxidation



(2) Formation of oxide layer by chemical reaction



(3) Growth of oxide layer with diffusion and chemical reactions

Oxidation – Cont'd

Rate of thermal oxidations:

Because of the extreme complexity of thermal oxidation, analytical methods for predicting the rate of this process is impossible. The following quasi-empirical formulas are used for the thickness of SiO_2 layer (x):

For small time, t:

$$x = \frac{B}{A}(t + \tau) \tag{8.9}$$

For larger time, t:

$$x = \sqrt{B(t + \tau)} \tag{8.10}$$

in which

$$\tau = \frac{\left[d_o^2 + 2D \frac{d_o}{k_s} \right] N_1}{2D N_o} \tag{8.11}$$

D = diffusivity of oxide in silicon, e.g. D = 4.4×10^{-16} cm^2/sec at 900°C.
do = initial oxide layer (~ 200 in dry oxidation, = 0 for wet oxidation)
k_s = surface reaction rate constant.
N_o = concentration of oxygen molecules in the carrier gas.
= 5.2×10^{16} molecules/cm^3 in dry O_2 at 1000°C and 1 atm.
= 3000×10^{16} molecules/cm^3 in water vapor at the same temperature and pressure.
N_1 = number of oxidizing species in the oxide.
= 2.2×10^{22} SiO_2 molecules/cm^3 with dry O_2,
= 4.4×10^{22} SiO_2 molecules/cm^3 in water vapor.

Oxidation – Cont'd

Rate of thermal oxidations – Cont'd

Determination of constant A and B in Eqs. (8.9) and (8.10):

For small time, t in Eq. (8.9):

$$\log\left(\frac{B}{A}\right) = aT' + b \qquad (8.12)$$

For larger time, t in Eq. (8.10):

$$\ln(B) = aT' + b \qquad (8.13)$$

where T' = 1000/T, with temperature T in Kelvin, K. Constant a and b are from the Table:

Constants	Coefficient (a)	Coefficient (b)	Conditions
Linear rate constant Eq. (8-12)	-10.4422 -10.1257 -9.905525 -9.92655	6.96426 6.93576 7.82039 7.948585	Dry O_2, E_a = 2 eV, (100) silicon Dry O_2, E_a = 2 eV, (111) silicon H_2O vapor, E_a = 2.05 eV, (110) silicon H_2O vapor, E_a = 2.05 eV, (111) silicon
Parabolic rate constant Eq. (8-13)	-14.40273 -10.615	6.74356 7.1040	Dry O_2, E_a = 1.24 eV, 760 Torr vacuum H_2O vapor, E_a = 0.71 eV, 760 Torr vacuum

Example 8.3

Estimate the thickness of the SiO_2 layer over the (111) plane of a "clean" silicon wafer, resulting from both "dry" and "wet" oxidation at 950°C for one and half hours.

Solution:

Since oxidation take place on a new "clean" silicon wafer, we can use the condition that $\tau = 0$. Thus, we may use:

$x = \frac{B}{A}t$ **for small time, and** $x = \sqrt{Bt}$ **for larger time.**

The constants, A and B in the above expressions are selected from Table 8.4 as follows:

	a	b	Conditions
Eq. (8-12)	-10.1257	6.9357	Dry O_2
Eq. (8-12)	-9.9266	7.9486	Wet steam
Eq. (8-13)	-14.4027	6.7436	Dry O_2
Eq. (8-13)	-10.6150	7.1040	Wet steam

Example 8.3 – Cont'd

Since we have T' = 1000/(950+273) = 0.8177, we obtained the constants B/A and B from Eqs. (8.12) and (8.13) as:

	Dry oxidation	Wet oxidation
B/A (μm/hr)	0.04532	0.6786
B (μm/hr)	0.006516	0.2068

The rates of oxidation in two conditions after 1.5 hours are thus obtained from the two equations available as:

	Dry oxidation (μm)	Wet oxidation (μm)
$x = \frac{B}{A} t$ for small time	0.068	1.018
$x = \sqrt{Bt}$ for larger time	0.0989	0.5572

We observe that wet oxidation results in much fast rates in oxidation than dry oxidation.

SiO_2 thickness by observations - A quick way to tell!

- **Both SiO_2 and Si_3N_4 layers have distinct color from the silicon substrates in which these layers grow.**
- **In the case of SiO_2 layers, they are essentially transparent but with distinct light refraction index from that of the silicon substrate.**
- **Consequently, when the surface is shone by the rays of white light one can view the surface exhibiting different colors corresponding to the layer's thickness.**
- **The color of the surface of a SiO_2 layer is the result of the interference of the reflected light rays.**
- **However, the same color may repeat with different layer thickness, as shown below:**

SiO_2 layer thickness (μm)	0.050	0.075	0.275 0.465	0.310 0.493	0.50	0.375	0.390
Color	Tan	Brown	Red violet	Blue	Green to Yellow green	Green yellow	Yellow

Chemical Vapor Deposition

- Chemical vapor deposition (CVD) is the most important process in microfabrication.

- It is used extensively for producing thin films by depositing many different kind of foreign materials over the surface of silicon substrates, or over other thin films that have already been deposited to the silicon substrate.

- Materials for CVD may include:
  (a) Metals: Al, Ag, Au, W, Cu, Pt and Sn.
  (b) Organic materials: Al_2O_3, polysilicon, SiO_2, Si_3N_4, piezoelectric ZnO, SMA TiNi, etc.

- There are three (3) available CVD processes in microfabrication:
  (a) APCVD: (Atmospheric-pressure CVD);
  (b) LPCVD (Low-pressure CVD), and
  (c) PECVD (Plasma-enhanced CVD).

- CVD usually takes place at elevated temperatures and in vacuum in high class clean rooms.

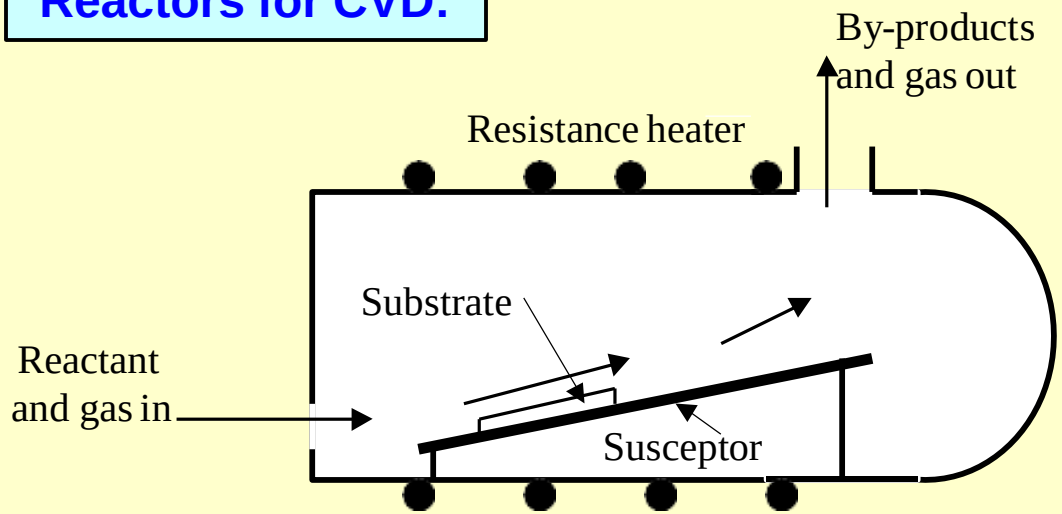
Chemical Vapor Deposition – Cont'd

Working principle of CVD:

- CVD involves the flow of a gas containing diffused reactants (normally in vapor form) over the hot substrate surface
- The gas that carries the reactants is called "*carrier gas*"
- The "diffused" reactants are foreign material that needed to be deposited on the substrate surface
- The carrier gas and the reactant flow over the hot substrate surface, the energy supplied by the surface temperature provokes chemical reactions of the reactants that form films during and after the reactions
- The by-products of the chemical reactions are then let to the vent
- Various types of CVD reactors are built to perform the CVD processes

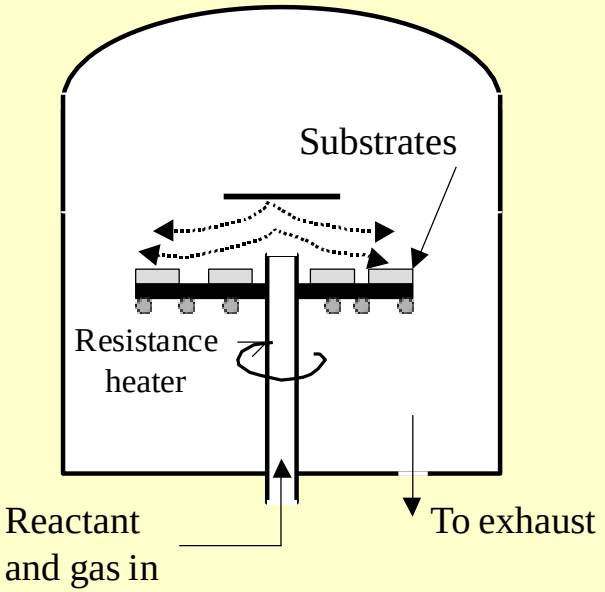
Chemical Vapor Deposition – Cont'd

Reactors for CVD:



Horizontal Reactor

Vertical Reactor



Chemical Vapor Deposition – Cont'd

Chemical reactions in CVD:

- **CVD of SiO_2 on silicon substrates:**

$$SiH_4 + O_2 \rightarrow \mathbf{SiO_2} + 2H_2 \qquad \text{at } 400 - 500^oC$$

Carrier gases are: O_2 (such as in the above reaction), NO, NO_2, CO_2 and H_2. The diffused reactant in the reaction is **Silane (SiH_4)** -a common reactant in CVD.

- **CVD of Si_3N_4 on silicon substrates:**

$$3SiH_4 + 4NH_3 \rightarrow \mathbf{Si_3N_4} + 12\ H_2 \qquad \text{at } 650 - 750^oC$$
$$3SiCl_4 + 4NH_3 \rightarrow \mathbf{Si_3N_4} + 12\ HCl$$
$$3SiH_2Cl_2 + 4NH_3 \rightarrow \mathbf{Si_3N_4} + 6HCl + 6H_2$$

- **CVD of polysilicon on silicon substrates:**

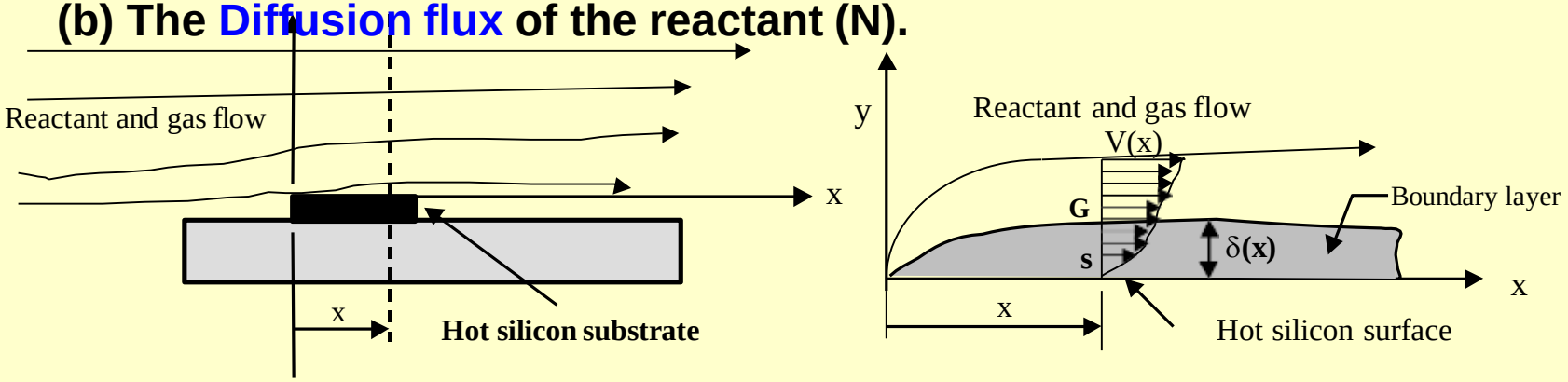
It is essentially a pyrolysis process of Silane at $600 - 650^oC$.

$$SiH_4 \rightarrow \mathbf{Si} + 2H_2$$

Chemical Vapor Deposition – Cont'd

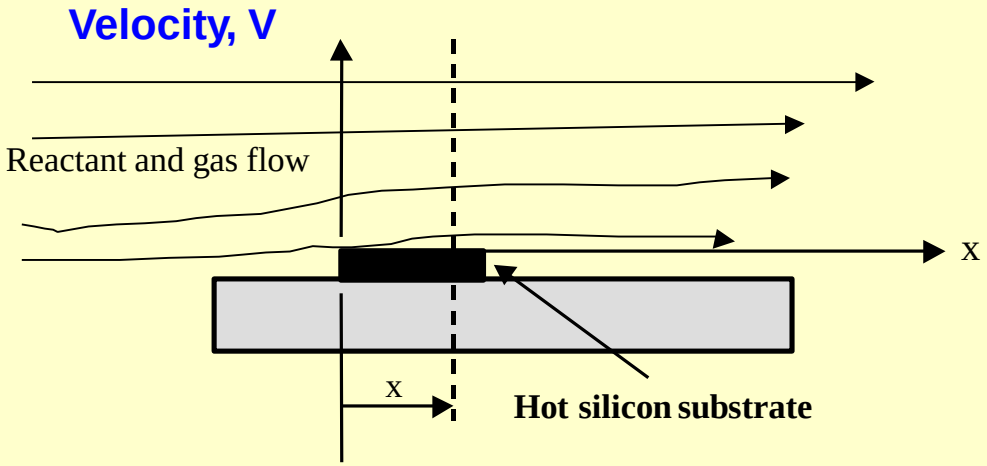
Rate of CVD Build-up:

- CVD is the principal technique for building the desired 3-D geometry of many MEMS and microsystems by means of thin film deposition.
- The rate of the build-up of these thin films obviously is a concern to process design engineers.
- Quantification of the rate of CVD is extremely complicated. A quasi-quantitative assessment of such rate of build-up may begin with the understanding of the physical-chemical principles on which CVD operates.
- Two major factors affect the rate of CVD:
  - (a) The velocity of carrier gas and the diffused reactant, as measured by the Reynold's number (Re) and the associated boundary layer (δ) thickness at the substrate-gas interface.
  - (b) The Diffusion flux of the reactant (N).



Chemical Vapor Deposition – Cont'd

Rate of CVD Build-up-Cont'd:



The Reynolds number:

$$R_e = \frac{\rho L V(x)}{\mu} \qquad (8.18)$$

where L = length of the substrate

Dynamic Viscosity (μ) of Carrier Gases Used in CVD Processes

Gas	Viscosity (micro poises, μP) @0°C	@490°C	@600°C	@825°C
Hydrogen, H_2	83	167	183	214
Nitrogen, N_2	153	337	-	419
Oxygen, O_2	189	400	-	501
Argon, Ar	210	448	-	563

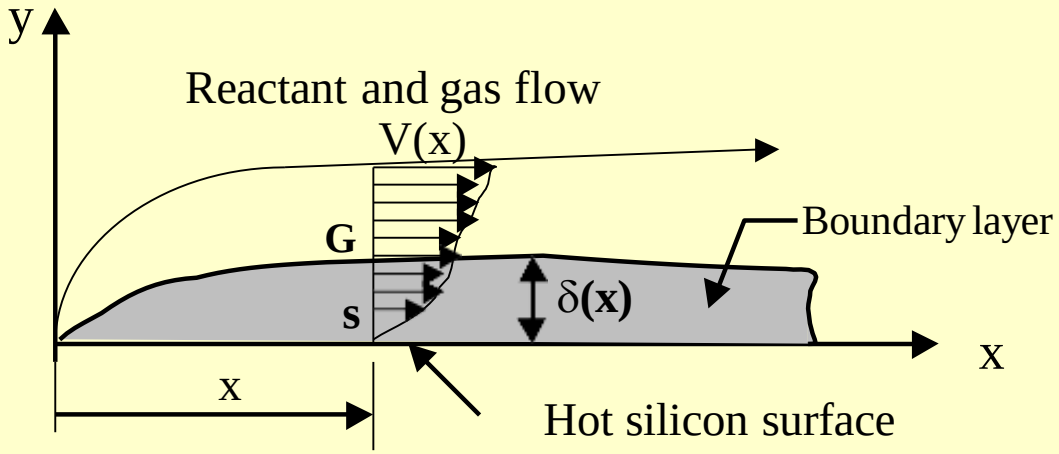
1 Poise (P) = 1 dyne-s/cm^2 = 0.1 N-s/m^2 = 0.1 Kg/m-s

Chemical Vapor Deposition – Cont'd

Enhanced CVD

The working principles of CVD process leads to the observations that the rates of CVD is proportional to the following physical parameters:

- **The temperature, $T^{3/2}$.**
- **The pressure of the carrier gas, P^{-1}.**
- **The velocity of gas flow, V^{-1}.**
- **The distance in the direction of gas flow, $x^{1/2}$, in which x is shown in Fig. 8-10 (b):**



Chemical Vapor Deposition – Cont'd

Enhanced CVD – Cont'd

Low-Pressure CVD (LPCVD)

Low-Pressure CVD (LPCVD):

From the previous observation, we may formulate the parameters that affect the rate of CVD:

$$r \propto \frac{(T^{1.5})(x^{0.5})(D)}{(P)(V)(\delta)}$$

A few possibilities exist to enhance the rate of CVD:

(1) To raise the process temperature, T would normally increase diffusivity, D. However, it will harm the substrate.

(2) To decrease the velocity, V may enhance the rate r, but also results in lower Reynolds number that will increase the boundary layer thickness, δ. These two effects may cancel out each other. So, it is not a positive option.

(3) This leaves with the last option to decrease the pressure of the gas, P with expectation to enhance the rate, r of the CVD.

Thus, LPCVD operates in vacuum at about 1 torr (1 mm Hg) has become a popular CVD process in microfabrication.

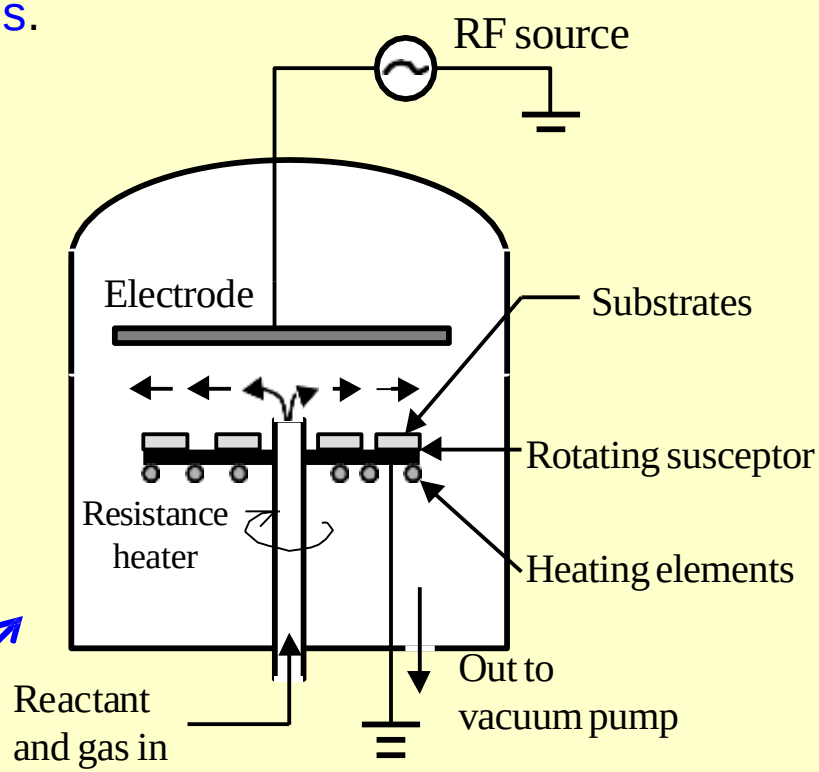
The CVD operates at atmospheric pressure is called APCVD.

Chemical Vapor Deposition – Cont'd

Enhanced CVD – Cont'd

Plasma Enhanced CVD (PECVD)

- Both APCVD and LPCVD operate at **elevated temperatures**, which often damage the silicon substrates..
- High substrate surface temperature is required to provide sufficient energy for diffusion and chemical reactions.
- The operating temperatures may be avoided if alternative form of energy supply can be found.
- CVD using **plasmas** generated from high energy **RF (radio-frequency) sources** is one of such alternative methods.
- This popular deposition method is called "Plasma Enhanced CVD" or **PECVD**.
- A typical PECVD reactor is shown:



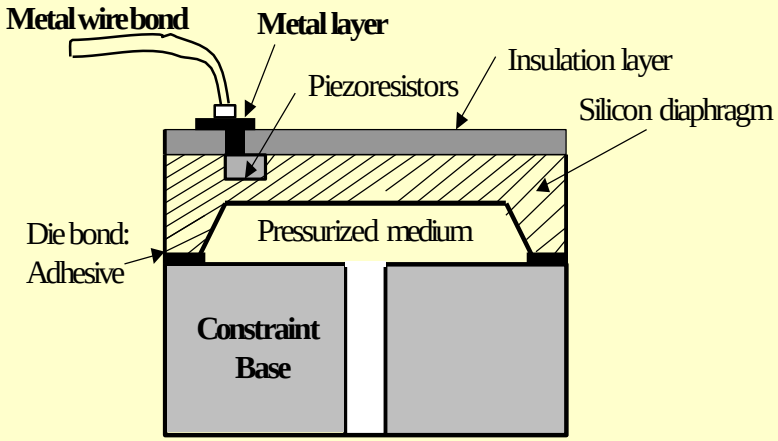
Chemical Vapor Deposition – Cont'd

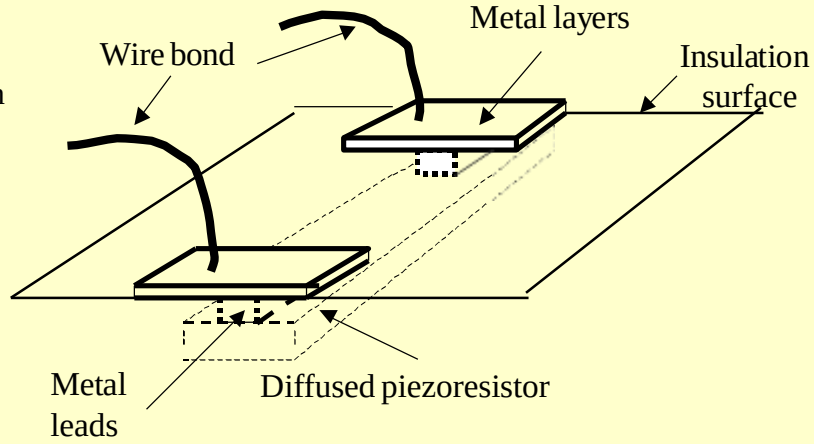
Summary and Comparison of 3 CVD Processes

CVD Process	Pressure/ Temperature	Normal Deposition Rates, (10^{-10} m/min)	Advantages	Disadvantages	Applications
APCVD	100-10 KPa/ 350-400°C	700 for SiO_2	Simple, high rate, low temperature	Poor step coverage, particle contamination	Doped and undoped oxides
LPCVD	1-8 Torr/ 550-900°C	50-180 for SiO_2 30-80 for Si_3N_4 100-200 for polysilicon	Excellent purity and uniformity, large wafer capacity	High temperature and low deposition rates	Doped and undoped oxides, silicon nitride, polysilicon, and tungsten.
PECVD	0.2-5 Torr/ 300-400°C	300-350 for Si_3N_4	Lower substrate temperature; fast, good adhesion.	Vulnerable to chemical contamination	Low-temperature insulators over metals, and passivation.

Sputtering

- Sputtering is a form of **Physical Vapor Deposition**.
- It is used to deposit thin **metal films** in the order of 100 A (1A = 10^{-10} m) onto the substrate surface.
- Metal films are used as electrical circuit terminals as illustrated below:

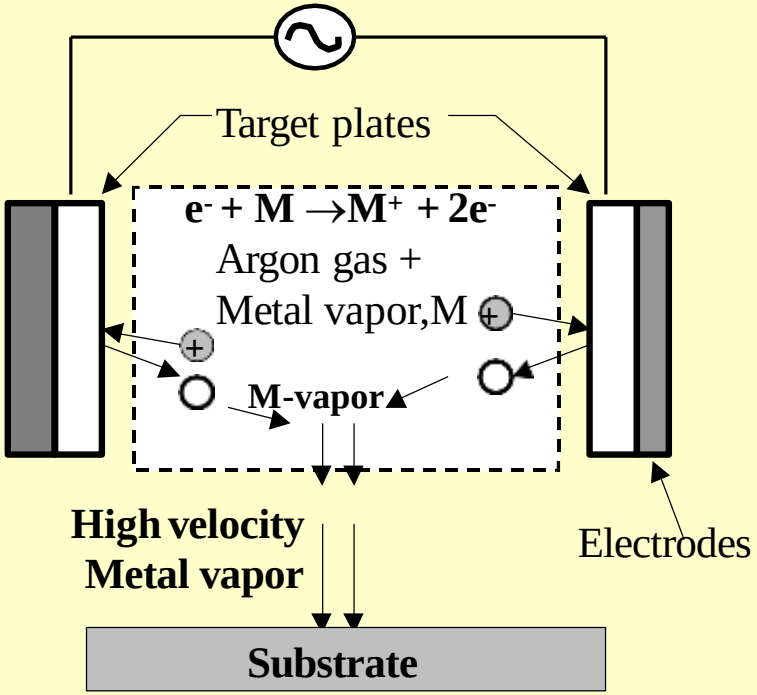




- Sputtering process is carried out with plasmas under very low pressure in **high vacuum** up to $5x10^{-7}$ torr and at **room temperature**.
- No chemical reaction is involved in the deposition process.

Sputtering – Cont'd

- **Metal vapor** is created by the plasma generated by the high energy RF sources, such as the one illustrated below.



- Inert **Argon gas** is used as the carrier gas for metal vapor.

- The metal vapor forms the metal films after condensation of the substrate surface.

Deposition by Epitaxy

- Both CVD and PVD processes are used to deposit dissimilar materials on the silicon substrate surfaces.
- Epitaxy deposition process is used to deposit **polysilicon** films on **silicon substrate** surfaces.
- Most polisilicons are doped pure silicon crystals randomly oriented. They are used to conduct electricity at desired locations on silicon substrates.
- This process is similar to CVD with carrier gas with **reactants that release the same material as the substrates.**
- One may deposit GaAs to GaAs substrates using this technique.
- There are four epitaxy deposition methods available.
- We will focus our attention on the popular "Vapor-phase epitaxy" (**VPE**) process.

Deposition by Epitaxy – Cont'd

The reactant vapors

Reactant vapors	Normal process temperature (^oC)	Normal deposition rate ($\mu m/min$)	Required energy supply (eV)	Remarks
Silane (SiH_4)	1000	0.1 – 0.5	1.6 – 1.7	No pattern shift
Dichlorosilane (SiH_2Cl_2)	1100	0.1 – 0.8	0.3 – 0.6	Some pattern shift
Trichlorosilane ($SiHCl_3$)	1175	0.2 – 0.8	0.8 – 1.0	Large pattern shift
Silicon tetrachloride ($SiCl_4$)	1225	0.2 – 1.0	1.6 – 1.7	Very large pattern shift

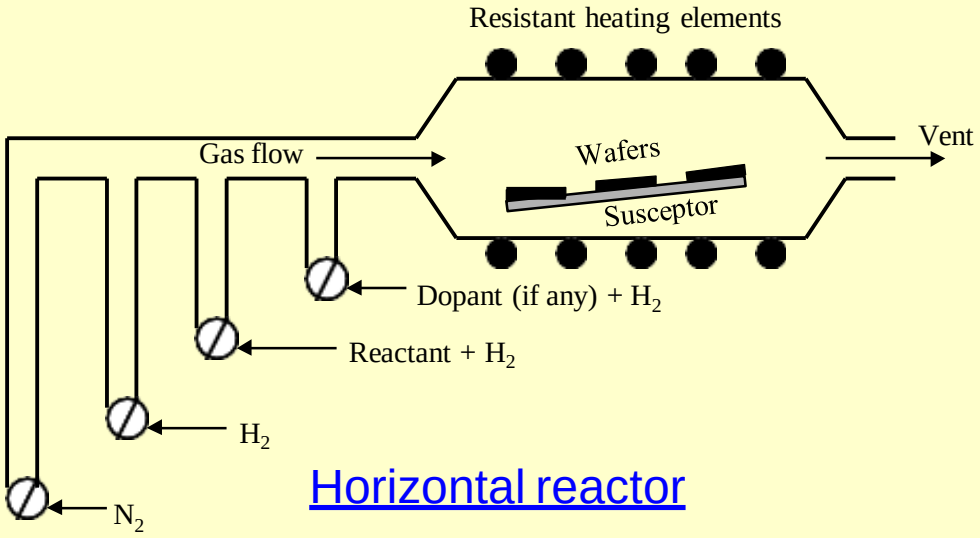
Typical chemical reaction:

$$SiH_4 \rightarrow \mathbf{Si}\ (\text{solid}) + 2H_2\ (\text{gas})$$

Deposition by Epitaxy – Cont'd

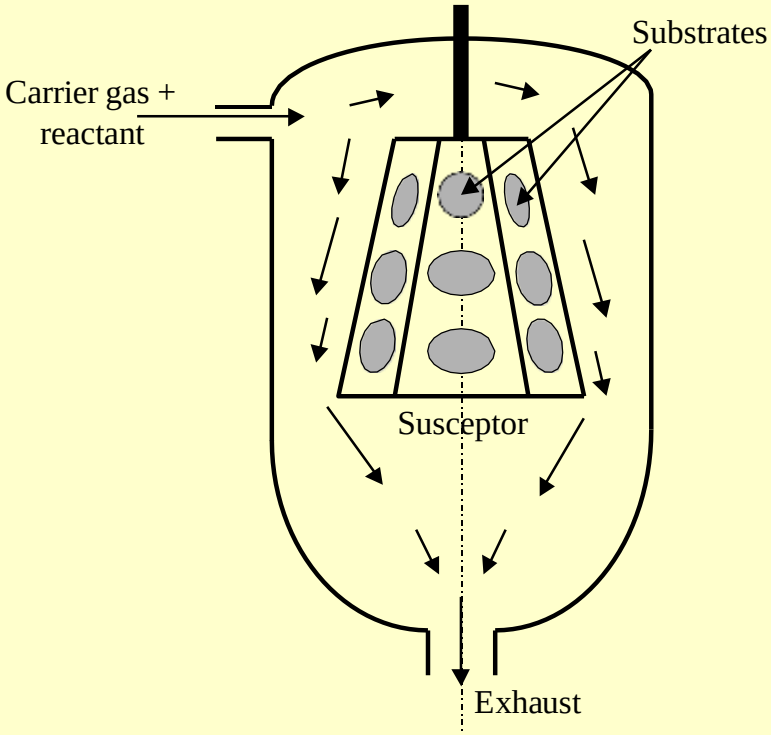
Reactors for epitaxy deposition

- Very similar to those used in CVD, except that many of the carrier gas used is **H_2**.
- For safety reason, **N_2** gas is used to drive out any O_2 gas in the system before the process begins.
- The two types of reactors are illustrated below:



Horizontal reactor

Vertical reactor



Etching

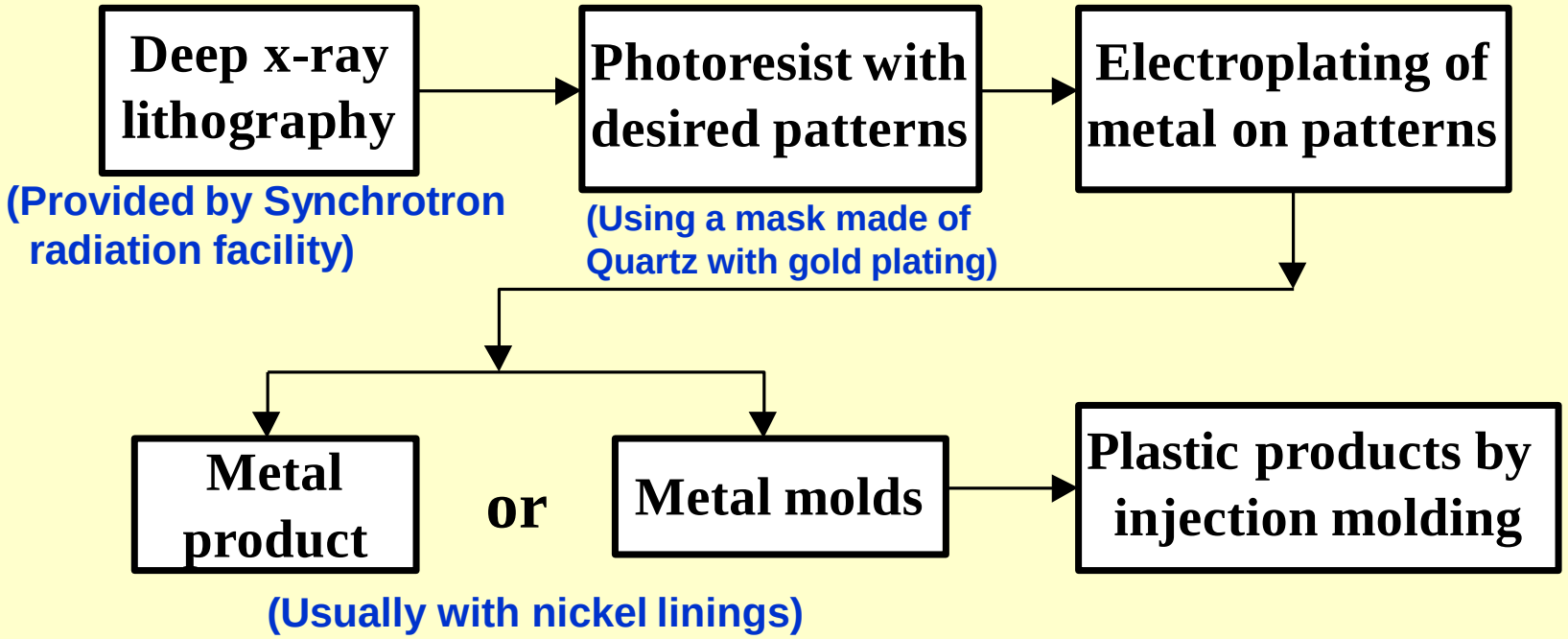
- MEMS and microsystems consist of components of 3-dimensional geometry.
- There are two ways to create 3-dimensional geometry:
  - by **adding** materials at the desired locations of the substrates using vapor deposition techniques, or
  - by **removing** substrate material at desired locations using the eticing methods.
- There are two types of etching techniques:
  - **Wet etching** involving the use of strong chemical solvents (**etchants**), or
  - **Dry etching** using high energy **plasmas**.
- In either etching processes, **masks** made of strong-resisting materials are used to protect the parts of substrate from etching.
- Both etching methods will be presented in detail in the subsequent chapter on Micromanufacturing.

The LIGA Process

- The term LIGA is an acronym for German term in "*Lithography* (Lithographie), *electroforming* (Galvanoformung), and *molding* (Abformung)".
- The technique was first developed at the Karlsruhe Nuclear Research Center in Karlsruhe, Germany.
- LIGA process is radically different from silicon-based micro manufacturing.
- The major difference is that LIGA can produce microstructures that have high aspect ratio.
- There is no restriction on using silicon or silicon compounds as substrate. Nickel is a common material for LIGA products.
- It is easier to be produced in large volumes.
- Major disadvantage of LIGA process is the requirement of special facility - Synchrotron radiation (X-ray) source, a very expensive facility.

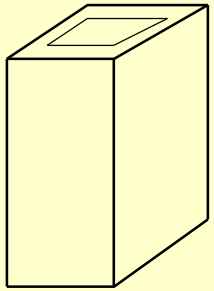
The LIGA Process – Cont'd

Major steps in LIGA process

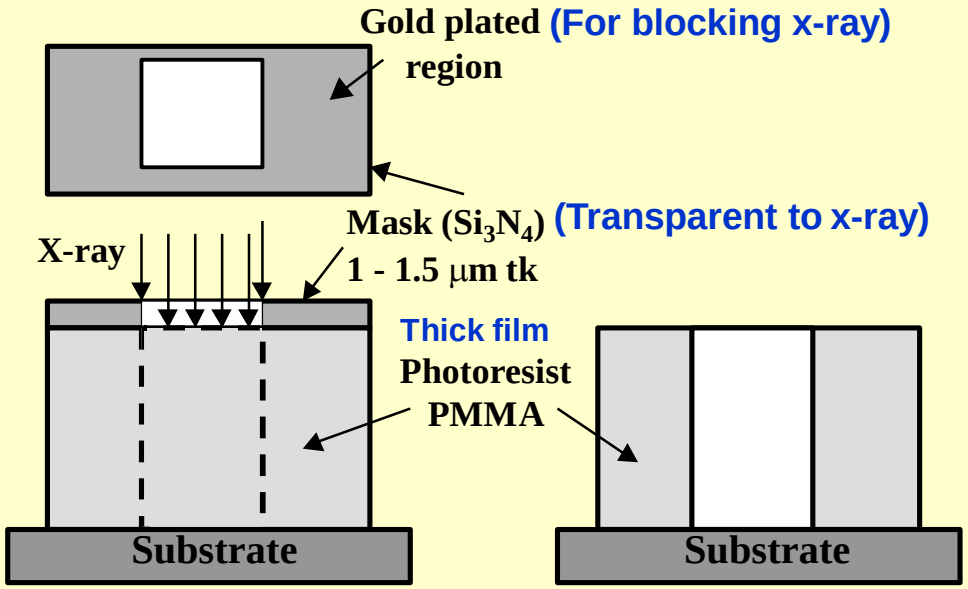


The LIGA Process – Cont'd

Fabrication of a square tube using LIGA

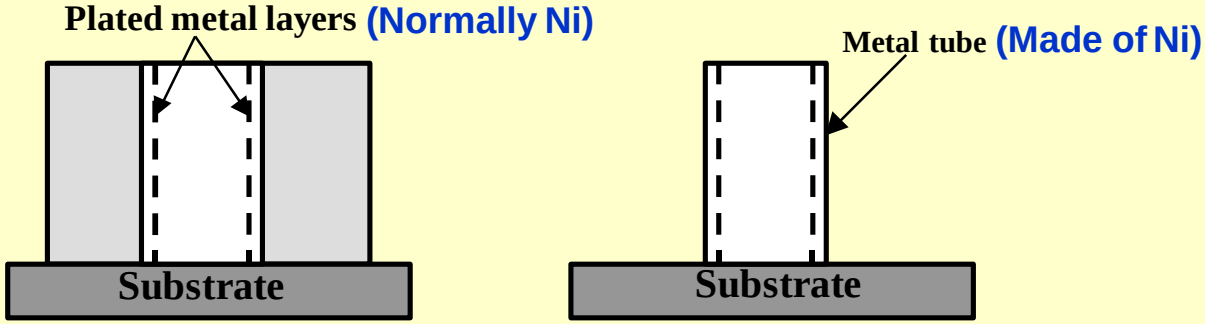


The desired product: a tube



(a) X-ray lithography

(b) Resist after lithography



(c) After electroplating

(d) After removing resist

The LIGA Process – Cont'd

Materials for substrates

- **Substrates in LIGA process must be electrical conductive to facilitate subsequent electroplating over photoresist mold.**
- **Metals such as: steel, copper plates, titanium and nickel, or**
- **Silicon with thin titanium or silver/chrome top layer; glass with thin metal layers.**

Photoresist materials

Basic requirements:

- Must be sensitive to x-ray radiation.
- Must have high resolution and resistance to dry and wet etching.
- Must have thermal stability up to 140oC.
- The unexposed part must be absolutely insoluble during development.
- Good adhesion to substrate during electroplating.
- PMMA appears most popular for LIGA process, but other polymers are available:

	PMMA	POM	PAS	PMI	PLG
Sensitivity	Bad	Good	Excellent	Reasonable	Reasonable
Resolution	Excellent	Reasonable	Very bad	Good	Excellent
Sidewall smoothness	Excellent	Very bad	Very bad	Good	Excellent
Stress corrosion	Bad	Excellent	Good	Very bad	Excellent
Adhesion on substrate	Good	Good	Good	Bad	Good

The LIGA Process – Ends

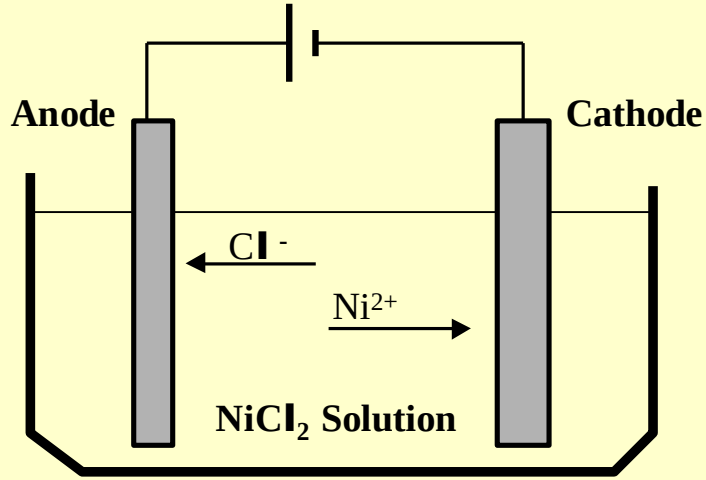
Electroplating

- The inner surfaces of the photoresist mold produced by X-ray lithography need to be plated with thin metal layers for securing permanent microstructure geometry.
- Metals available for the plating are: Ni, Cu, Au, NiFe and NiW.
- In the case of plating with Ni, the process is:

- Nickel ions (Ni^{2+}) are produced from electrolysis of $NiC\ell_2$ solution.

- They are attracted to the electrons at the cathode:

$$Ni^{2+} + 2e^- \rightarrow Ni$$



- There could be H^+ ions presence at the same cathode in the process.
- These H+ ions may form H_2 bubbles on the cathode, and thus Ni plate.
- Proper control of the pH in the solution is important to mitigate this effect.

Initial Design Considerations

- Design constraints:
  - Customer demands: applications; product specifications; operating environments
  - Time to market
  - Environmental conditions: temperature; humidity; chemical; optical.
  - Size and weight limitations
  - Life expectance
  - Availability of fabrication facility
  - Costs