ACS College of Engineering

Department of Biomedical Engineering

HDL pre lab questions (2015-2016)

Cycle-1

1. What is truth table?

2. Which gates are called universal gates?

3. Define HDL?

4. What is the difference b/w HDL and software language?

5. Define Entity and architecture?

6. Define identifiers.

7. A basic 2-input logic circuit has a HIGH on one input and a LOW on the other input, and the output is HIGH. What type of logic circuit is it?

8. Write the sum and carry expression for half and full adder.

Cycle-2

1.Define mux and demux.

2. Write their applications.

3. What is the relationship b/w input lines and select lines.

4. Design 4:1 mux and 1:4 demux.

5. write brief notes on case statement.

6. Write the difference b/w if and while statement

7.What is difference b/w encoder and data selector.

8. What is the difference b/w decoder and data distributor.

9. Give the applications of encoder and decoder.

10. Write short notes on " with – select" statement.

Cycle-3

1. Describe the main difference between a gated S-R latch and an edge-triggered S-R flip-flop.

2. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

3. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

4. What is use of characteristic and excitation table?

5. What are synchronous and asynchronous circuits?

6. How many flip flops due you require storing the data 1101?

7. What is propagation delays set up time and hold time?

8. How to generate clock signal in VHDL?

9. What are the different wait statements?

Cycle-4

1.How does synchronous counter differ from asynchronous counter?

2. How many flip-flops do you require to design Mod-6 counter.

3. What are the different types of counters?

4. What are the different types of shift registers?

5. How many f/fs are needed for n-bit counter?

6. What is meant by universal shift register?

7. What is ALU?

8. What are the operations can be done by using ALU?

9. What are the predefined Attributes?

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HDL Lab pre lab questions (2016-2017)

Cycle-1

1. What is truth table?

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6. Define identifiers.

7. A basic 2-input logic circuit has a HIGH on one input and a LOW on the other input, and the output is HIGH. What type of logic circuit is it?

8. Write the sum and carry expression for half and full adder.

9. Briefly explain the behavioral model?

10. Expand IEEE?

11.What is significance of library 1164?

Cycle-2

1.Define mux and demux and Write their applications.

2. What is the relationship b/w input lines and select lines.

3. Design 4:1 mux and 1:4 demux.

4. write brief notes on case statement.

5. Write the difference b/w if and while statement

6.What is difference b/w encoder and data selector.

7. What is the difference b/w decoder and data distributor.

8. Give the applications of encoder and decoder.

9. Write short notes on “with – select” statement.

10. Explain signal assignment statements?

11. Write syntax for Loop statement.

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1. Describe the main difference between a gated S-R latch and an edge-triggered S-R flip-flop.

2. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

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4. What are synchronous and asynchronous circuits?

5. How many flip flops due you require storing the data 1101?

6. What is propagation delays set up time and hold time?

7. How to generate clock signal in VHDL?

8. What are the different wait statements?

9.write characteristic expression for JK F/F?

Cycle-4

1. How does synchronous counter differ from asynchronous counter?

2. How many flip-flops do you require to design Mod-8 counter.

3. What are the different types of counters?

4. What are the different types of shift registers?

5. What is meant by universal shift register?

6. What is ALU?

7. What are the operations can be done by using ALU?

8. What are the predefined Attributes?

9.Explain cathode seven segment display?

Content beyond the syllabus:

1) **Write a verilog program for 4:16 decoder?**
2) **Write VHDL structural program for 2:4 decoders?**

1) **Write a verilog program for 4:16 decoder?**

```
module decoder_4x16 (d_out, d_in);

   output [15:0] d_out;
   input [3:0]   d_in;
   parameter tmp = 16'b0000_0000_0000_0001;

assign d_out = (d_in == 4'b0000) ? tmp   :
               (d_in == 4'b0001) ? tmp<<1:
               (d_in == 4'b0010) ? tmp<<2:
               (d_in == 4'b0011) ? tmp<<3:
               (d_in == 4'b0100) ? tmp<<4:
               (d_in == 4'b0101) ? tmp<<5:
               (d_in == 4'b0110) ? tmp<<6:
               (d_in == 4'b0111) ? tmp<<7:
               (d_in == 4'b1000) ? tmp<<8:
               (d_in == 4'b1001) ? tmp<<9:
               (d_in == 4'b1010) ? tmp<<10:
               (d_in == 4'b1011) ? tmp<<11:
               (d_in == 4'b1100) ? tmp<<12:
               (d_in == 4'b1101) ? tmp<<13:
               (d_in == 4'b1110) ? tmp<<14:
               (d_in == 4'b1111) ? tmp<<15: 16'bxxxx_xxxx_xxxx_xxxx;

endmodule
```

2) **Write VHDL structural program for 2:4 decoders?**

```
entity Decoder_2to4 is
   port( A0, A1: in std_logic;
         D0, D1, D2, D3 : out std_logic);
end Decoder_2to4;
--
architecture func of Decoder_2to4 is
   component andGate is         --import AND Gate entity
      port( A, B : in std_logic;
                F : out std_logic);
   end component;

   component notGate is         --import NOT Gate entity
      port( inPort : in std_logic;
           outPort : out std_logic);
   end component;
```

```
   signal invOut0, invOut1 : std_logic;

begin
   GI1: notGate  port map(A0, invOut0);
   GI2: notGate  port map(A1, invOut1);

   GA1: andGate  port map(invOut1, invOut0, D0);
   GA2: andGate  port map(invOut1, A0, D1);
   GA3: andGate  port map(A1, invOut0, D2);
   GA4: andGate  port map(A1, A0, D3);
end func;
```

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8. Briefly explain the behavioral model?

9. Expand IEEE?

Cycle-2

1.Define mux and demux and Write their applications.

2. What is the relationship b/w input lines and select lines.

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4. Write the difference b/w if and while statement

5.What is difference b/w encoder and data selector.

6. What is the difference b/w decoder and data distributor.

7. Write short notes on “with – select” statement.

8. Explain signal assignment statements?

9. Write syntax for Loop statement.

Cycle-3

1. Describe the main difference between a gated S-R latch and an edge-triggered S-R flip-flop.

2. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

3. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

4. What are synchronous and asynchronous circuits?

5. What is propagation delays set up time and hold time?

6. How to generate clock signal in VHDL?

8.write characteristic expression for JK F/F?

Cycle-4

1. How does synchronous counter differ from asynchronous counter?

2. How many flip-flops do you require to design Mod-8 counter.

3. What are the different types of counters?

4. What are the different types of shift registers?

5. What is meant by universal shift register?

7. What are the operations can be done by using ALU?

8. What are the predefined Attributes?

9.How speed and direction of stepper motor can be controlled?

Content beyond the syllabus:

1) **Write HDL code to generate different waveform Sawtooth using DAC change the frequency and amplitude.**
2) **Write VHDL structural program for 4:1 MUX?**

1)Write HDL code to generate different waveform Sawtooth using DAC change the frequency and amplitude.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sawtooth is
port (clk : in std_logic;
    wave_out : out std_logic_vector(7 downto 0);
    reset :in std_logic
   );
end sawtooth;

architecture Behavioral of sawtooth is

signal count : integer := 0;

begin

process(clk,reset)
begin
if(reset = '1') then
  count <= 0;
elsif(rising_edge(clk)) then
  if(count = 255) then
     count <= 0;
  else
     count <= count + 1;
  end if;
end if;
end process;

wave_out <= conv_std_logic_vector(count,8);

end Behavioral;
```

3) **Write VHDL structural program for 2:1 MUX?**

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity multiplexer2_1 is
    port(
        a : in STD_LOGIC;
        b : in STD_LOGIC;
        sel : in STD_LOGIC;
        dout : out STD_LOGIC
        );
end multiplexer2_1;

architecture multiplexer2_1_arc of multiplexer2_1 is
component and2 is
   port (a : in STD_LOGIC;
         b : in STD_LOGIC;
         dout : out STD_LOGIC
         );
end component and2;

component or2 is
   port (a : in STD_LOGIC;
         b : in STD_LOGIC;
         dout : out STD_LOGIC
         );
end component or2;

component not1 is
   port (a : in STD_LOGIC;
         dout : out STD_LOGIC
         );
end component not1;

signal m : std_logic;
signal n : std_logic;
signal o : std_logic;


begin

   u0 : and2 port map (a,m,n);
   u1 : and2 port map (sel,b,o);
   u2 : or2 port map (n,o,dout);
   u3 : not1 port map (sel,m);


end multiplexer2_1_arc;
```